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Design Of Operational Amplifiers And Utilizing Sic Jfet For Analog Design

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DESIGN OF OPERATIONAL AMPLIFIERS AND UTILIZING SIC JFET FOR ANALOG DESIGN

By

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SIC JFET FOR ANALOG DESIGN

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Demand for capable and reliable semiconductor and fabrication technology for high temperature and power electronics applications has been increasing in recent years. Silicon Carbide (SiC), as a wide bandgap compound semiconductor, demonstrates superior characteristics such as high thermal conductivity, high breakdown voltage, and long-lasting reliable operation at elevated temperature. SiC-based circuits and systems are capable to offer significant performance enhancements to various applications. Integrated power management units and conversion modules in HEVs, integrated sensors for aircraft engines, development of small-sized portable power generators are among many applications that require reliable circuits with long-lasting functional lifetime. Nevertheless, there are numerous challenges associated with the design and fabrication of SiC-based circuits.

The aim of this research is to practically design and implement novel operational amplifiers (opamps) based on Vertical Channel 4H-SiC JFET (SiC JFET) that can be

utilized as sub-circuits of integrated SiC JFET-based circuits and systems. Recently, SiC power JFET-based power management units were developed that deploy non-SiC JFET-based circuits for analog signal processing, driving, and control, because all SiC JFET-based circuits were not available for full integration. However, utilizing SiC JFET for analog design (in order to close the mentioned gap) exhibits significant design challenges, even at room temperature. These fundamental challenges are low intrinsic gain, the requirement to limit the gate to source voltage range, and restrictions on utilizing channel length as a design parameter due to fabrication complexity. These challenges must be successfully overcome at room temperature, before moving towards high temperature SiC JFET-based analog design.

The main objective of this dissertation is to establish a design base, overcome the challenges, demonstrate the feasibility, and present all SiC JFET-based opamps that are designed for gain, CMRR, and overall performance. Before attempting to design, both Enhancement and Depletion Mode SiC JFETs are characterized, analyzed, and modeled for simulation. Unique and reliable opamp configurations are presented that take design requirements into account, use threshold voltage instead of channel length as a design parameter, and employ gain enhancement techniques while obtaining maximum possible bandwidth. The final opamps are fabricated and tested and the results show that the objective is accomplished.

Key words: analog, high temperature, jfet, operational amplifier, sic

DEDICATION

I dedicate this dissertation to my family.

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I would like to extend my gratitude and appreciation to my family with their unconditional support and my advisor Dr. Michael S. Mazzola for his time, commitment, guidance, and financial support that enabled me to complete my doctoral program. I sincerely thank my committee members Dr. Raymond S. Winton, Dr. Yaroslav Koshka, and Dr. Marshall Molen for providing valuable insight and guidance.

While I was working at SemiSouth Laboratories, Inc. as an analog design engineer, this research started on January 2006 for one year duration. At that time, Dr. Mazzola was the Vice President for Technology and Chief Technology Officer for SemiSouth on a leave of absence from Mississippi State University. Afterwards, this research moved to Center for Advanced Vehicular Systems (CAVS) of Mississippi State University, starting on January 2008. During the time at SemiSouth, preliminary modeling of the SiC JFETs, simulation, and SiC JFET-based circuit design were performed. After fabrication of the actual SiC JFET devices, the research continued at CAVS by conducting comprehensive device characterization and completing the device SPICE modeling along with conducting simulation, design, fabrication, and test of the SiC JFET-based operational amplifiers.

I am grateful to many people in the Department of Electrical and Computer Engineering at Mississippi State University, SemiSouth Laboratories, and CAVS who

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CHAPTER I

MOTIVATION AND CHALLENGES

1.1 Introduction

1.1.1 Silicon Carbide Material

Silicon Carbide (SiC) is one of the hardest materials and is a robust semiconductor with crystal lattice structure identical to silicon and diamond. Half of the SiC's crystal lattice sites are occupied by silicon atoms and the other half by carbon atoms. SiC material has advantages over silicon and diamond. In high temperature applications, its electronic properties are superior to silicon and unlike diamond it can be manufactured [1]. SiC is not only an excellent choice for harsh environment and high temperature electronics, but it is also one of the most promising materials for harsh environment mechanical microsystems and MEMS in various applications.

MEMS-based gas turbine engines are currently under development for use as button-sized portable power generators [2]. Power densities expected for these micro engines require very high rotor peripheral speed and high combustion gas temperature. These harsh requirements need a qualified material with high strength. SiC has been chosen as the most promising material for such an environment. Evidently, fabrication technology of SiC material is still in its infancy, but qualification of SiC material for

various harsh environment electronics and mechanical systems suggests that it is realistic to imagine opportunities where fully integrated electronics side by side with mechanical micro-systems are fabricated in SiC in the future.

1.1.2 Material Properties of SiC

SiC band gap energy (3.2 eV in 4H-SiC) is almost three times higher than the silicon (1.1 eV). The electron hole pair generation rate decreases exponentially as band gap increases; therefore, the intrinsic carrier concentration in SiC (figure 1.1) and the

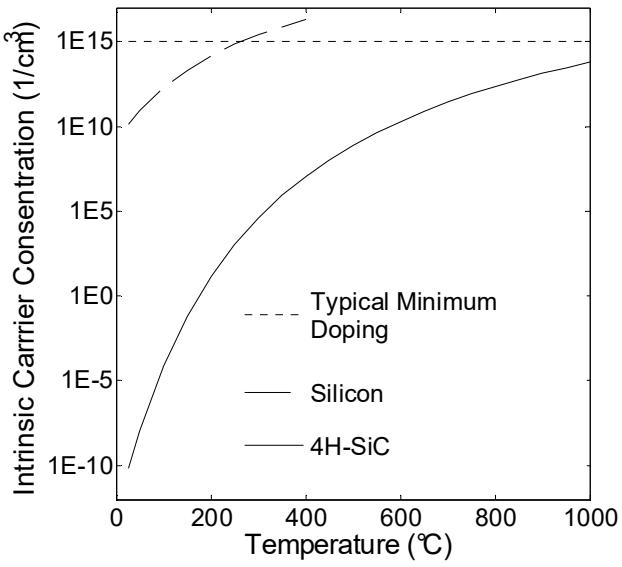


Figure 1.1. Intrinsic carrier concentration increases in silicon and 4H-SiC as temperature increases. As long as intrinsic carrier concentration is less than the minimum doping, devices are functional. Limit for silicon is as low as 250°C and for 4H-SiC is over 1000°C.

thermal leakage current is sixteen orders of magnitude lower than silicon. As temperature increases, leakage current also increases and it becomes problematic above 250°C for

silicon-based circuits compared to 1000°C for SiC-based circuits. SiC material and fabrication technology is rapidly growing, and it is anticipated that SiC-based circuits will reliably operate at the junction temperature above 300°C. In fact, [3], [4] have reported reliable operation of SiC-based circuits at 500°C for over seven thousand hours. Thermal stability of SiC is another superior material property compared to silicon that contributes to reliable high temperature operation of the SiC devices.

1.1.3 Electronic Properties of SiC

In applications where both power electronics and high temperature operation are required SiC devices have significant advantages over silicon devices. Issues such as high internal junction temperature and leakage, which are produced by self heating at ambient temperature above 200°C, disqualify silicon for such harsh applications [5]. Other important parameters in power electronics are critical electric field for avalanche breakdown and thermal conductivity. Table 1.1 [6] shows Breakdown Field of 3 MV/cm and Thermal Conductivity of 4.9 W/cm-K for 4H-SiC, which are five and over three

Table 1.1. Electronic properties of five selected semiconductors, after [6].

Properties	Si	GaAs	6H-SiC	4H-SiC	3H-SiC
Bandgap (eV)	1.1	1.42	3.0	3.2	2.3
Breakdown Field at 10^{17} cm^{-3} (MV/cm)	0.6	0.6	3.2	3.0	> 1.5
Electron Mobility at 10^{16} cm^{-3} (cm^2/V-s)	1100	6000	370	800	750
Hole Mobility at 10^{16} cm^{-3} (cm^2/V-s)	420	320	90	115	40
Thermal Conductivity (W/cm-K)	1.5	0.5	4.9	4.9	5.0
Saturated Electron Drift Velocity (cm/s)	10^7	10^7	2×10^7	2×10^7	2.5×10^7

times higher than in silicon, respectively. In table 1.2 [5], various harsh environment applications are listed, where SiC devices are superior and more qualified to be deployed over Bulk Silicon (BS) silicon and Silicon on Insulator (SOI).

Table 1.2. Semiconductor technologies used for various high temperature and power electronics applications, after [5].

High Temperature Electronics Application	Peak Ambient	Chip Power	Current Technology	Future Technology
Automotive:				
Engine Control Electronics	150 °C	< 1 kW	BS & SOI	BS & SOI
On-cylinder & Exhaust System	600 °C	< 1 kW	NA	WBG
Electric suspension & Brakes	250 °C	> 10 kW	BS	WGB
Hybrid Electric Vehicle/Electric	150 °C	> 10 kW	BS	WGB
Turbine Engine				
Sensors, Telemetry, Control	300 °C	< 1 kW	BS & SOI	SOI & WBG
	600 °C	< 1 kW	NA	WBG
Electric Actuation	150 °C	> 10 kW	BS & SOI	WBG
	600 °C	> 10 kW	NA	WBG
Spacecraft				
Power management Units	150 °C	> 1 kW	BS & SOI	WBG
	300 °C	> 10 kW	NA	WBG
Venus & Mercury Exploration	550 °C	~ 10 kW	NA	WBG
Industrial				
High Temperature Processing	300 °C	< 1 kW	SOI	SOI
	600 °C	< 1 kW	NA	WBG
Deep-Well Drilling Telemetry				
Oil & Gas	300 °C	< 1 kW	SOI	SOI & WBG
Geothermal	600 °C	< 1 kW	NA	WBG

1.2 SiC Device Technologies

1.2.1 SiC MOSFETs

There has been a considerable progress in SiC MOSFET device development where a number of analog and digital circuits have been demonstrated to date [7], [8], [9], and [14]. SiC MOSFET technology has shown a performance limit for high temperature

application above 250°C. One of the failure parameters in SiC MOSFETs at high temperature is degradation of gate oxide. In SiC MOSFET, when there is sufficient applied electric field at elevated temperature, carriers can enter oxide from semiconductor and propagate through it. This phenomenon causes damages and leaves trapped charges in oxide and interfaces between oxide and semiconductor [5]. Therefore, gate oxide dielectric of SiO_2 is not suitable for SiC devices in high temperature application and should be avoided, especially, when high electric filed is present [1]. Additionally, growth of defect free gate oxide dielectric on SiC is a key technological challenge [10]. Interface defects and poor characteristics of grown SiO_2 over SiC material shows higher fixed charge and high interface state densities [6]. As a result, channel mobility of both N-type and P-type SiC MOSFETs are significantly degraded. Table 1.3 [9] shows an example of measured SiC MOSFET parameters. NMOS shows low and PMOS shows very poor mobility performance that makes deployment of PMOS in circuit design, unlikely. SiC NMOS experiences a high threshold voltage (V_{th}) variation of –7.6 mV/°C over the range of 25°C to 350°C. Moreover, high temperature circuit drift instability at 350°C in a SiC MOSFET has been discovered and reported [8].

Table 1.3. SiC NMOS and PMOS parameters variation versus temperature in [9].

Temperature (°C)	$V_{th\text{-}N}$ (V)	$V_{th\text{-}P}$ (V)	μ_N (cm^2/V-s)	μ_P (cm^2/V-s)
25	3.3	-4.2	19.7	4.5
100	2.4	-3.6	19	7.7
200	1.6	-3.4	26	8
300	1.2	-3.2	23.6	7.3

1.2.2 SiC MESFETs

SiC MESFETs have also been considered for high temperature electronic circuits. The main problems with the SiC MESFET are current instability due to trapping effects [11], high leakage current at high temperature, and poor interface contact between N-channel and P-type buffer layer at elevated temperature [12].

1.2.3 SiC JFETs

The SiC JFET compares favorably to the SiC MOSFET and the MESFET. The JFET does not require a critical gate dielectric to function; however, it maintains high input impedance, even though, not as high as SiC MOSFETs. The SiC JFET offers higher channel mobility, operates at junction temperatures above 250°C (the upper limit for SiC MESFET and MOSFET), has smaller variation in V_{th} over a wide temperature range, and is believed to be less susceptible to long term high temperature reliability and stability problems. It is also easier to fabricate than either the SiC MOSFET or the SiC MESFET.

"The SiC JFET" refers to the Vertical Channel 4H-SiC JFET throughout this dissertation. It illustrates superior electronic properties compared to the SiC MOSFET. However, it exhibits a few design challenges that need to be addressed. For example, low intrinsic gain, low Gate to Source Voltage Range (GSVR), and a restricted ability to utilize Channel Length (CL) as a design parameter due to fabrication complexity are the fundamental challenges. In fact, both the SiC JFET and the MESFET share the same challenges of low intrinsic gain and low GSVR compared to the SiC MOSFET. GSVR is an important concept, which will widely be used throughout this dissertation, and it is

only meaningful for JFET and MESFET devices. GSVR is a range of applicable voltage to the gate to source of a JFET or MESFET that maintains safe operation of the device in "ON" state. Lower limit of the GSVR is determined by V_{th} and upper limit is bounded by the built in voltage of the gate to source P-N junction. For protection of the device, upper limit should stay below 2.5 V (4H-SiC bandgap is 3.2 eV) in room temperature and 2 V in 350°C in order not to forward bias the junction. Increasing gate to source voltage above 2.5 V will forward bias the P-N junction and will cause excessive forward leakage current and device overheating. Therefore, for an Enhancement Mode (EM) SiC JFET (V_{th} is greater than zero), maximum GSVR is less than 2.5 V in room temperature. With the silicon JFET, the maximum GSVR is less than 0.6 V making EM silicon JFET device, unusable. The low GSVR requirement creates a great design challenge in both analog and digital domains, but it is more serious in analog domain.

Table 1.4 provides a list of advantages and disadvantages of using SiC JFET for room and high temperature analog design among other SiC counterparts. Operational amplifiers (opamps), as the main building elements for analog design, are subject of research in SiC devices. Opamps have been reported based on SiC MOSFET [8], [9], and [14] and SiC MESFET [12] devices. However, no opamps are fabricated and reported to date that utilize all SiC MESFET or SiC JFET transistors without using passive components in their main stages. Therefore, this dissertation intends to utilize EM and Depletion Mode (DM) SiC JFETs to present design and fabrication of all SiC JFET transistor based opamps.

Table 1.4. Comparison of the SiC JFET (Vertical Channel 4H-SiC JFET) technology with SiC MOSFET and SiC MESFET technologies.

	SiC Devices		
Comparison Criteria	SiC MOSFET	SiC MESFET	SiC JFET
Gate oxide requirement to function	Yes	No	No
Gate oxide limitation on the functionality of device in high temperature	Yes	No	No
Poor ohmic contact to the backgate region	N/A	Yes	N/A
Failure above 250°C and high electric field	Yes	Yes	No
Long term reliability and functionality problem at high temperature	Yes	Yes	No
Reported instability at high temperature	Yes	Yes	No
Wide range of V_{th} variation based on temperature	Yes	No	No
Fabrication difficulty	Yes	Yes	No
Leakage current	Higher	Higher	Low
Electron mobility	Low	Higher	Higher
Transconductance	Low	Higher	Higher
V_{th} variation due to process variation (a design constraint)	Lower	Lower	High
Low intrinsic gain (a design constraint)	Yes	Yes	Yes
Low GSVR requirement (a design constraint)	No	Yes	Yes
Using V_{th} for design instead of CL if the channel is vertical (a design constraint)	N/A	Yes	Yes
Reported all SiC transistor based opamps	Yes	**No**	**No**

1.3 Literature Review

1.3.1 SiC MOSFET Opamp

1.3.1.1 N. S. Rebello et al.: 6H silicon carbide MOSFET modeling for high temperature analogue integrated circuits (25°C to 500°C)

Rebello et al. [14] focus primarily on modeling temperature variations on large and small signal parameters of SiC N-type MOSFET devices and assesses its suitability for high temperature circuits. Parameters are V_{th}, leakage current, body-bias effect, small signal transconductance, and output conductance. For instance, the V_{th} of a SiC NMOS is extrapolated using transconductance against gate voltage in the temperature range of 25°C to 300°C. Below 200°C the slope of V_{th} variation in SiC NMOS is –10mV/K, which is a considerably larger than the measured V_{th} variation of the SiC JFET [13].

Based on the measured device parameters, an NMOS opamp is simulated and designed. The opamp is expected to work in the range of 25°C to 500°C, but the observation of gate to drain leakage through the gate oxide and pin to pin package leakage above 300°C reveals the fault mechanism associated with SiC MOSFETs and the practical limitations of packaging at high temperature. The opamp is designed using all NMOS transistors, since PMOS was not available for CMOS design. Measured parameters of SiC NMOS reveals the fact that mobility in SiC NMOS is about fifteen times lower than for silicon at 250°C, which severely limits the bandwidth, because $f = \mu \cdot V_{DSa}\ /\ \ $. Unity gain frequency is presented by "f", mobility by "μ", overdrive voltage or drain to source saturation voltage by "V_{DSat}", and device channel length by

"L". The overall work suggests that the SiC NMOS transistor is not an ideal candidate for high temperature applications, especially for temperature above 250°C.

1.3.1.2 J. Chen et al.: Design of a Process Variation Tolerant CMOS Opamp in 6H-SiC Technology for High Temperature Operation

A SiC CMOS opamp [9] is designed by Chen et al. that operates over the range of 27°C to 300°C. The opamp is simulated using extracted SPICE parameters from a 5 μm SiC CMOS P-well technology. Performance of the designed SiC CMOS opamp at 300°C indicates that the circuit design techniques are well employed for such a result. However, device parameters measured in this work show very poor channel mobility, especially with the P-type SiC MOSFET, and high sheet resistance. Consequently, unity-gain frequency, slew rate, and output resistance are degraded. This work also concludes that SiC devices are capable of high temperature application, but the key issues with gate oxide specific to SiC MOSFETs need to be resolved before they can be reliably deployed in high temperature circuits.

1.3.2 SiC MESFET Opamp

1.3.2.1 M. Tomana et al.: A Hybrid Silicon Carbide Differential Amplifier for 350°C Operation

Tomana et al. [12] design an opamp using SiC MESFET pairs. The amplifier is tested in the temperature range of 25°C to 350°C. Open loop gain of the opamp is greater than 60 dB and Common Mode Rejection Ratio (CMRR) is greater than 55 dB over the temperature range. Measured transconductance of the MESFET pairs versus temperature

shows superior performance as compared to SiC NMOS. Based on the measured device characteristics SPICE parameters are extracted using GaAs MESFET model. An opamp is designed using two differential amplifier (diffamp) stages with a source degenerated structure for stability over a range of temperature.

The main concerns using SiC MESFETs in high temperature application are their instability and poor interface contact effect between the N-channel and the P-type buffer layer. The authors illustrate the specific problem due to poor ohmic interface contact that they encounter in the second differential pair (second stage) of the opamp. Due to the poor ohmic contact to the backgated region, a charge coupling to the floating backgate causes distortion in the I-V curves of the SiC MESFET. The charge coupling effect decreases with increasing temperature as a direct result of junction leakage in higher temperature. Instability of SiC MESFETs at higher temperature and reliability issues at the interface contact suggest that they are not reliable devices for high temperature circuits, up to now.

1.3.3 SiC JFET Amplifier Circuit

1.3.3.1 J. Jung et al.: Simulated Performance of SiC-Based Opamp at High Temperature

In this paper [15], a SiC N-type JFET-based opamp is simulated. SPICE parameters are extracted using a JFET model developed for the simulation. Performance of the simulated opamp is compared to its counterpart in silicon NMOS TSMC 0.18 μm technology. The open loop gain of the SiC N-type JFET opamp demonstrates better performance in temperature variation when compared to a silicon opamp. The SiC JFET

has lower drift in V_{th} than silicon NMOS; therefore, the SiC JFET opamp has less drift in bias points and stays functional over a larger temperature variation. The authors brief their reasons for investigating the SiC N-type JFET for opamps, which are low channel motilities and the imperfect gate oxide interface in the SiC MOSFET and high temperature instability in the SiC MESFET.

1.4 Motivation

Considering SiC material and electronic properties, SiC JFETs offer superior characteristics among other SiC counterparts. Superior and more importantly reliable electronic circuits for harsh environment with long-lasting functional lifetime are undoubtedly highly demanding requirements. Recent progress and development in SiC-based electronic systems and mechanical microsystems such as SiC motor drive inverters [16], high temperature sensors [17], and MEMS require reliable analog subsystems for signal processing. For instance, a SiC motor drive inverter [16] employs SiC power JFET transistors for power switching and driving the motor, while SOI-based circuits are used to drive and control the power JFETs. The reasoning behind using SOI-based circuitry is that no reliable fully SiC JFET-based analog and control circuits are available. In order to close the gap, the most essential analog subsystem "opamps" must be realized and introduced using SiC JFET transistors. Eventually, technology and fabrication improvements will lead to a full integration of all subsystems to present suitable control circuitry. A summary of the motivations for designing SiC JFET-based opamps can be highlighted as: 1) SiC is a robust and promising semiconductor with

excellent material and electronic properties for high temperature and power electronics application. 2) SiC MOSFET-based opamps have unreliable and poor overall performance characteristics above 250°C. SiC MOSFET devices suffer from imperfect SiC/SiO_2 interface. Poor device characteristics such as low surface channel mobility and high sheet resistance are repeatedly reported. 3) SiC MESFET has poor ohmic contact to the backgate region; therefore, an opamp designed with the MESFET shows performance degradation and instability at elevated temperature. 4) SiC JFET shows superior device characteristics compare to both the SiC MOSFET and the SiC MESFET. It is more reliable and has longer functional life time at elevated temperature. On the other hand, it possesses great circuit design challenges. 5) A SiC JFET-based opamp is expected to be a robust and reliable with long lasting functional lifetime that has superior overall performance in high temperature and power electronics application. 6) Novel all SiC JFET-based opamps are highly demanding for integration of all subsystems in power electronics and high temperature environment. For instance, integration of the signal processing and control subsystems (which require opamps as the main elements) with power switching modules will enable the entire system to operate in the same environment and temperature that will greatly enhance the performance of the systems and reduce the size of the overall system significantly.

1.5 Dissertation Statement

Superior performance of the SiC semiconductor (Vertical Channel 4H-SiC JFET or simply SiC JFET in this dissertation) for high temperature and harsh environment is

known. However, utilizing SiC JFET for analog design exhibits significant design challenges, even at room temperature. Low intrinsic gain, the requirement to limit the GSVR, and restrictions on utilizing CL as a design parameter due to fabrication complexity are the fundamental challenges. First, these challenges must successfully be overcome in room temperature, before moving towards high temperature SiC JFET-based analog design. The main objective of this dissertation is to establish a design base, overcome the challenges, demonstrate the feasibility, and present all SiC JFET-based opamps that are designed for gain, CMRR, and overall performance. Before attempting to design, EM and DM SiC JFETs are characterized, analyzed, and modeled for simulation. Unique and reliable opamp configurations are presented that take design requirements into account, use V_{th} instead of CL as a design parameter, and employ gain enhancing design techniques while obtaining maximum possible bandwidth. The final opamps are fabricated and tested and the results are reported in the related chapters.

1.6 Organization of the Dissertation

Chapter two will present SiC JFET device characterization and modeling for the temperature range of 27°C to 400°C. Small signal characteristic are also illustrated in the same temperature range. SiC JFET-based analog blocks and performance analysis will be discussed in chapter three. This chapter presents a design base and essentials for deploying DM and EM SiC JFETs for analog design. Chapter four will realize a four stage opamp that is designed for gain and CMRR performance. Chapter five presents a

more universal design of an opamp for overall performance that is suitable for a conventional temperature range. Chapter six provides the conclusions to the entire work.

CHAPTER II

SILICON CARBIDE JFET DEVICE CHARACTERIZATION AND MODELING OVER THE TEMPERATURE RANGE OF 27°C to 400°C

2.1 Introduction

A suitable SPICE model to support simulation of SiC JFET based analog circuit plays an essential role in the circuit design process. Since our emphasis is analog circuit analysis and design appropriate to the SiC JFET, rather than device-specific modeling, previously reported GaAs FET level five model [18] is adopted, which is a built-in model in SPICE and simulation tools. The similarity between the current to voltage behavior of the two compound semiconductor devices (GaAs FET and SiC JFET) allows us to apply the model and obtain a quite accurate result. Two types of SiC JFET devices have been fabricated "normally on" that is a DM device with negative V_{th} and "normally off" that is an EM device with positive V_{th}. In this chapter, both EM and DM devices are characterized and modeled in the temperature range of 27°C up to 400°C. At the end of this chapter, small signal characteristics of an EM SiC JFET in the same temperature range are presented. For analog design at elevated temperature, these characteristics and their variations are essential design parameters.

2.2 SiC JFET Devices

A conceptual device structure of a SiC JFET (Vertical Channel 4H-SiC JFET) [13] with the Channel Length (CL) of 2 µm, Channel Width (CW) or Finger Width (FW) of 2 mm, and Finger Length (FL) of 1.1 µm to 1.5 µm is shown in figure 2.1. From the CW, it can be realized that these devices are fabricated for high current and power electronics applications. Total CW of 2 mm is sum of the parallel arrays of the FWs shown in SEM image of figure 2.2(a). Both EM and DM devices that are used throughout the dissertation share exactly the same device structure and geometry except different FLs. Devices with FL of 1.1 µm are EMs, and longer ones towards 1.5 µm are DMs. No other device design parameters and fabrication detail were available to the author, since

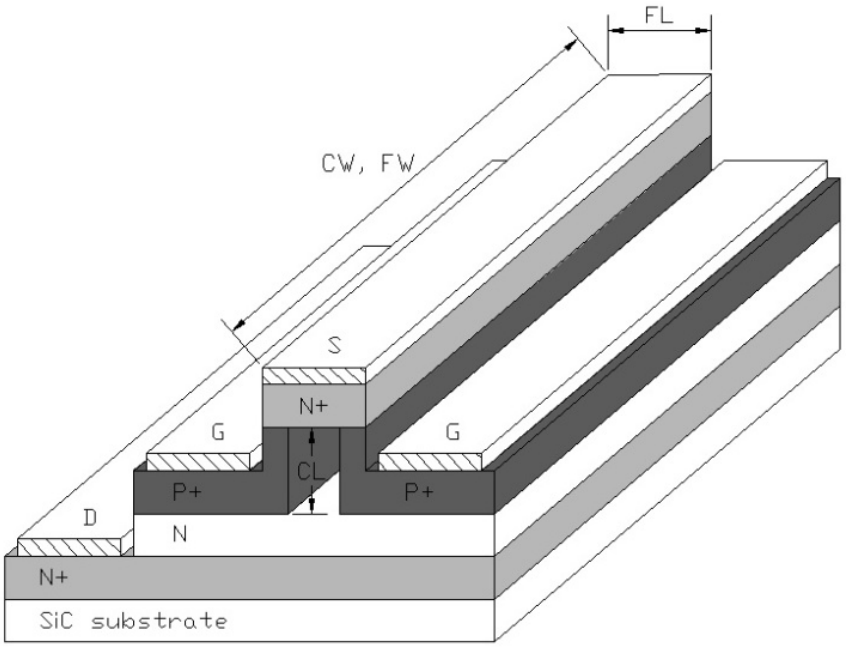
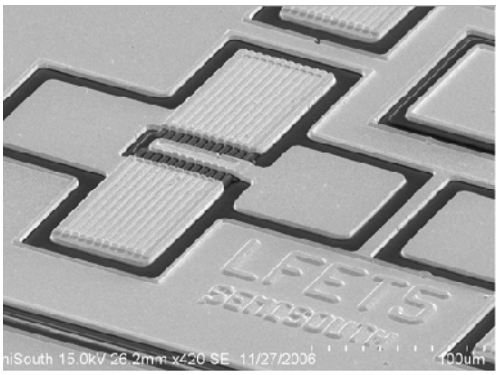
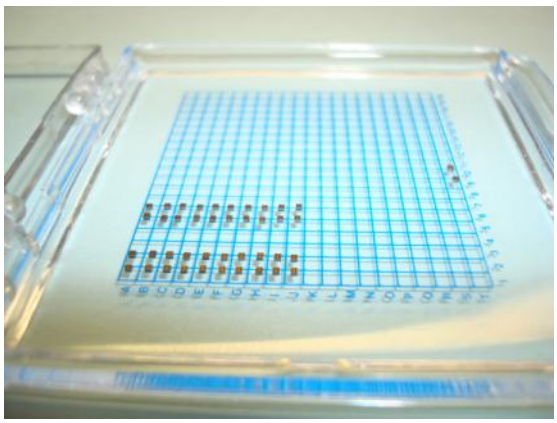


Figure 2.1. Device structure of a fabricated 4H-SiC JFET. Channel Length (CL) = 2 µm, Channel Width (CW) = 2 mm, and Finger Length (FL) = 1.1 µm to 1.5 µm (sizes are not in scale).

the devices are SemiSouth Laboratories' intellectual properties. Figure 2.1 also reveals an important point that the CL of the devices are vertical, which implies that fabricating number of these devices with multiple CLs all on the same die is a very complicated task; therefore, utilizing CL as a design parameter for analog circuits becomes quite restricted. This issue is compensated using V_{th} as a design parameter, which will to be discussed in chapter three. Figure 2.2(b) shows a number of EM and DM SiC JFETs after fabrication. There are four transistors in each die that are characterized and modeled.



(a)



(b)

Figure 2.2. (a) SEM image of a fabricated 4H-SiC JFET. (b) Fabricated dies.

2.2.1 Device Modeling at 27°C

Level five GaAs FET model [18] based on the equivalent circuit model shown in figure 2.3 defines cutoff, saturation region, and I_{gs} vs. V_{gs} in equations (1), (2), and (3) respectively. Summary of the parameters used in the equations are listed in table 2.1 [18]. SPICE parameters with temperature dependency are illustrated with (T), and are shown in equations (4) to (8). In order to visually evaluate the modeling and its accuracy, an EM device with V_{th} of +0.54 V is characterized and modeled at room temperature. I_{ds} vs. V_{ds} and I_{ds} vs. V_{gs} curves of the device are illustrated in figure 2.4 and 2.5. Comparing measured curves (doted lines) with modeled curves (solid lines), accuracy of the modeling can be evaluated. Figures 2.6, 2.7(a) and (b) are also representative of a measured and modeled curves of a DM device with V_{th} of –0.68 V at room temperature. In the modeling process, curves are modeled slightly worse than actual measurements in order to avoid overestimation in the simulation. For instance, output resistances of the modeled curves are slightly lower than the actual measurements from the devices.

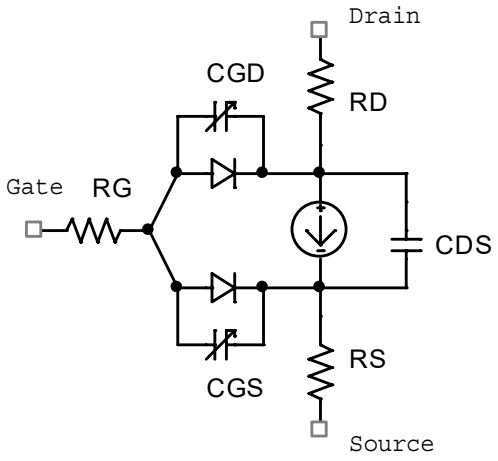


Figure 2.3. Equivalent circuit model for SiC JFETs.

In the cutoff region:

$$V_{ds} \geq 0,\ V_{gs} - V_{th}(T) + \gamma(T) \cdot V_{ds} \leq 0,\ \&\ N_g - N_d \cdot V_{ds} = 0 \Rightarrow I_D(T) = 0 \qquad (1)$$

In the linear and saturation region:

$$V_{ds} \geq 0,\ V_{gs} - V_{th}(T) + \gamma(T) \cdot V_{ds} > 0,\ \&\ N_g - N_d \cdot V_{ds} \neq 0$$

$$\Rightarrow I_D(T) = \frac{\beta(T) \cdot V_g^Q \cdot \dfrac{\alpha(T) \cdot V_{ds}}{\sqrt{1 + [\alpha(T) \cdot V_{ds}]^2}}}{1 + \delta(T) \cdot V_{ds} \cdot \beta(T) \cdot V_g^Q \cdot \dfrac{\alpha(T) \cdot V_{ds}}{\sqrt{1 + [\alpha(T) \cdot V_{ds}]^2}}} \qquad (2)$$

$$Where:\ V_g(T) = Q \cdot V_s(T) \cdot \ln\left[e^{\frac{V_{gs} - V_{th}(T) + \gamma(T) \cdot V_{ds}}{Q \cdot V_s(T)}} + 1 \right],$$

$$V_s(T) = [N_g + N_d \cdot V_{ds}] \cdot \left[\frac{kT}{q} \right],$$

$$Also:\ I_{gs}(T) = I_s(T) \cdot \left[e^{\frac{q.Vgs}{n \cdot kT}} - 1 \right] \qquad (3)$$

$$I_s(T) = I_s \cdot e^{\left[\frac{T}{T_{nom}} - 1 \right] \cdot \left[\frac{q \cdot E_g}{n \cdot kT} \right]} \cdot \left[\frac{T}{T_{nom}} \right]^{\frac{X_{ti}}{N}} \qquad (4)$$

$$V_{th}(T) = V_{th} + V_{th}' \cdot [T - T_{nom}] \qquad (5)$$

$$\alpha(T) = \alpha \cdot 1.01^{\alpha' \cdot [T - T_{nom}]} \qquad (6)$$

$$\beta(T) = \beta \cdot 1.01^{\beta' \cdot [T - T_{nom}]} \qquad (7)$$

$$\gamma(T) = \gamma + \gamma' \cdot [T - T_{nom}] \qquad (8)$$

Table 2.1. Summary of the model parameters and description.

Parameters (units)	Description
$T\ (K)$	Temperature
$V_{th}(T)\ (V)$	Threshold voltage at T (K)
$\gamma(T)\ (V^{-1})$	Threshold shifting parameter at T (K)
$N_g\ (-)$	Subthreshold slop gate parameter
$N_d\ (V^{-1})$	Subthreshold slop drain pull parameter
$\beta(T)\ (A/V^Q)$	Transconductance parameter at T (K)
$Q\ (-)$	Power-law parameter
$\alpha(T)\ (V^{-1})$	Knee voltage parameter at T (K)
$\delta(T)\ (V)$	Output feedback parameter at T (K)
$\gamma(T)\ (V^{-1})$	Threshold shifting parameter at T (K)
$k\ (eV \cdot K^{-1})$	Boltzmann's constant
$q\ (C)$	Charge of an electron
$I_S(T)\ (A)$	Gate diode saturation current at T (K)
$n\ (-)$	Gate diode ideality factor
$T_{nom}\ (K)$	Temperature at 300 (K)
$I_S\ (A)$	Gate diode saturation current at T = 300 K
$E_g\ (V)$	Barrier height
$X_{ti}\ (-)$	temperature exponent
$V_{th}\ (V)$	Threshold voltage at 300 K
$V_{th}^{'}\ (V/°C)$	Threshold voltage coefficient
$\alpha\ (V^{-1})$	Knee voltage parameter at 300 K
$\alpha^{'}\ (\%/°C)$	Temperature coefficient
$\beta\ (A/V^{-Q})$	Transconductance parameter
$\beta^{'}\ (\%/°C)$	Temperature parameter
$\gamma\ (V^{-1})$	Threshold shifting parameter
$\gamma^{'}\ (V^{-1})$	Temperature coefficient

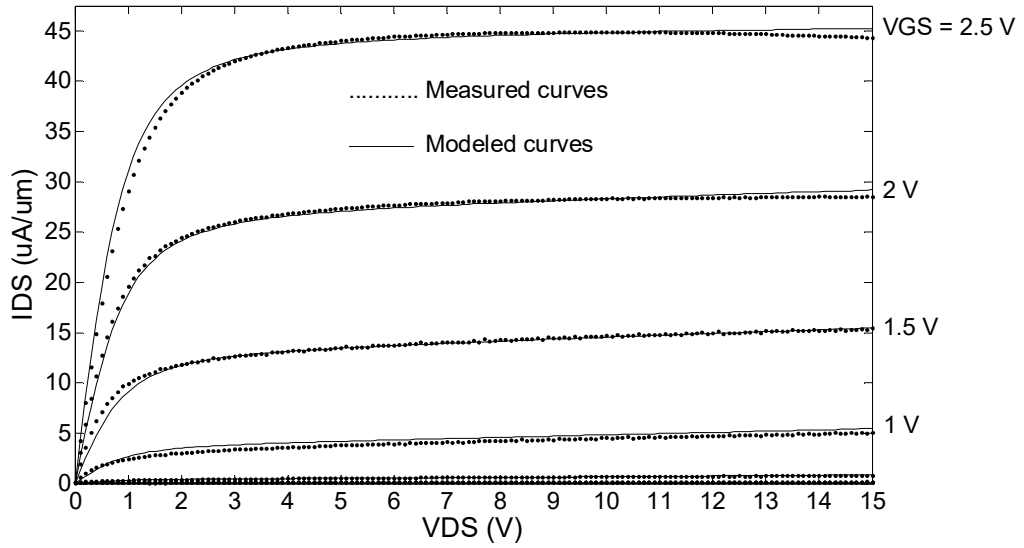


Figure 2.4. Measured and modeled I_{ds} vs. V_{ds} curves of an EM SiC JFET with V_{th} of +0.54 V, CW = 2 mm, and CL = 2 μm.

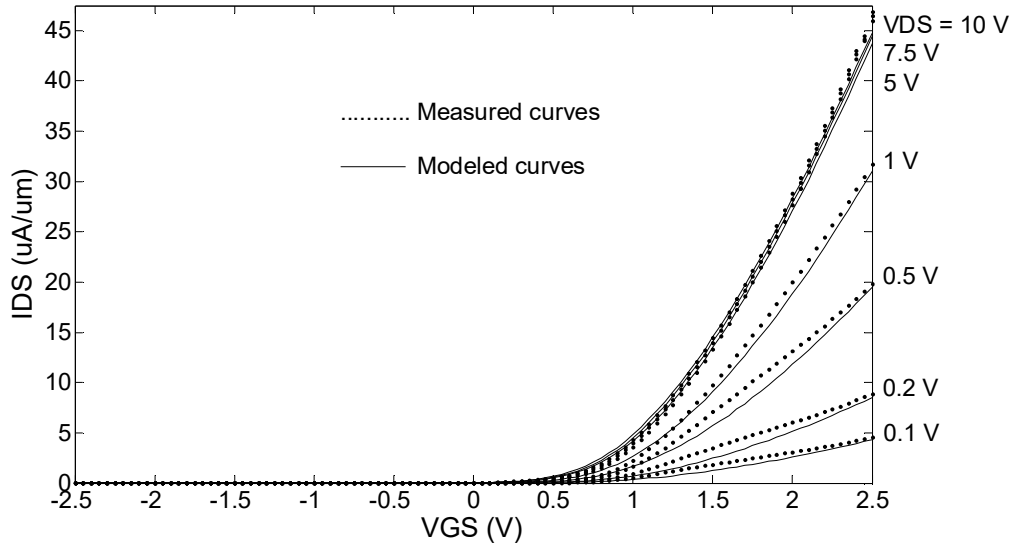


Figure 2.5. Measured and modeled I_{ds} vs. V_{gs} curves of an EM SiC JFET with V_{th} of +0.54 V, CW = 2 mm, and CL = 2 μm.

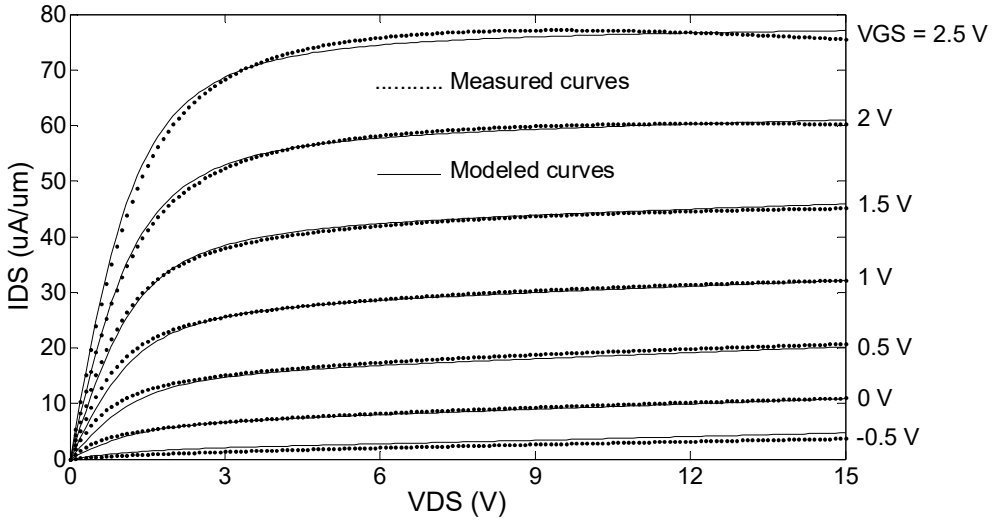
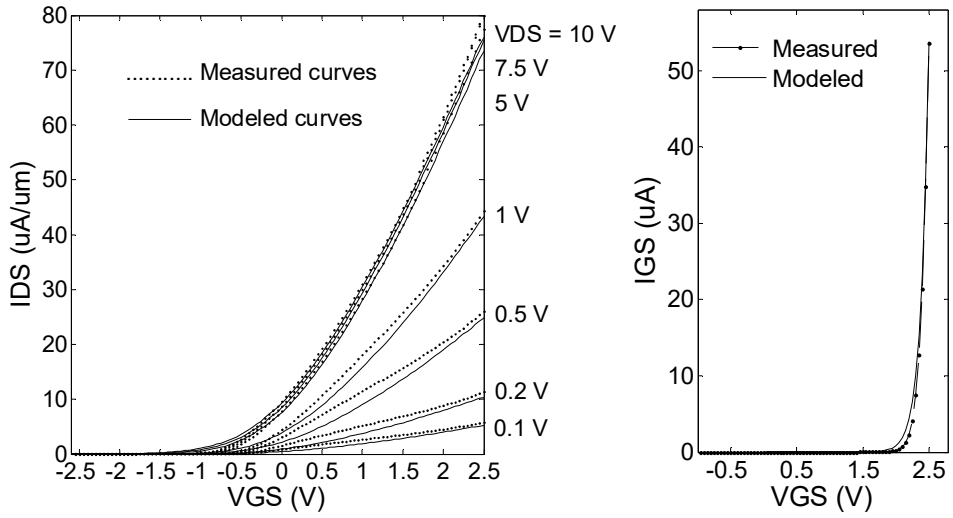


Figure 2.6. Measured and modeled I_{ds} vs. V_{ds} curves of a DM SiC JFET with V_{th} of –0.68 V, CW = 2 mm, and CL = 2 μm.



(a) (b)

Figure 2.7. Measured and modeled (a) I_{ds} vs. V_{gs} and (b) I_{gs} vs. V_{gs} curves of a DM SiC JFET with V_{th} of –0.68 V, CW = 2 mm, and CL = 2 μm.

2.2.2 Device Modeling over the Range of 27°C to 400°C

SiC JFET devices are modeled up to 400°C equipping simulation tools with SPICE model to simulate circuits at elevated temperature. Hence, measurements are conducted at 27°C, 100°C, and up to 400°C with 50°C increments. As a sample, measured characteristics and modeling of an EM device with V_{th} of 0.43 V at 27°C, 150°C, 250°C, and 400°C are illustrated in figures 2.8 to 2.13. Figures 2.8 to 2.11 show I_{ds} vs. V_{ds} curves from 27°C to 400°C. As moving toward higher temperature, it can be seen that amplitude of the drain current decreases, so is the accuracy of the model. This model is developed for conventional temperature applications; therefore, it requires some additional developments, especially around the V_{th} region. Figures 2.9 to 2.11 illustrate larger deviations between measured and modeled curves around V_{th} at higher temperature. In figure 2.12, drain current of the device decreases at elevated temperature by 74.4% similar to figures 2.8 to 2.11. In contrast, gate to source current in figure 2.13 is increasing in the same temperature range (with V_{gs} = 2.5 V) by 39.5 times. Both of the variations are undesirable and introduce design challenges for high temperature analog design.

Our focus in this dissertation is analog design at conventional temperature range dealing with the design challenges imposed by SiC JFET devices. The aim is to present circuits that are tolerant to large parameter variations. However, this model has been providing us with realistic simulation and reasonable results even at higher temperature.

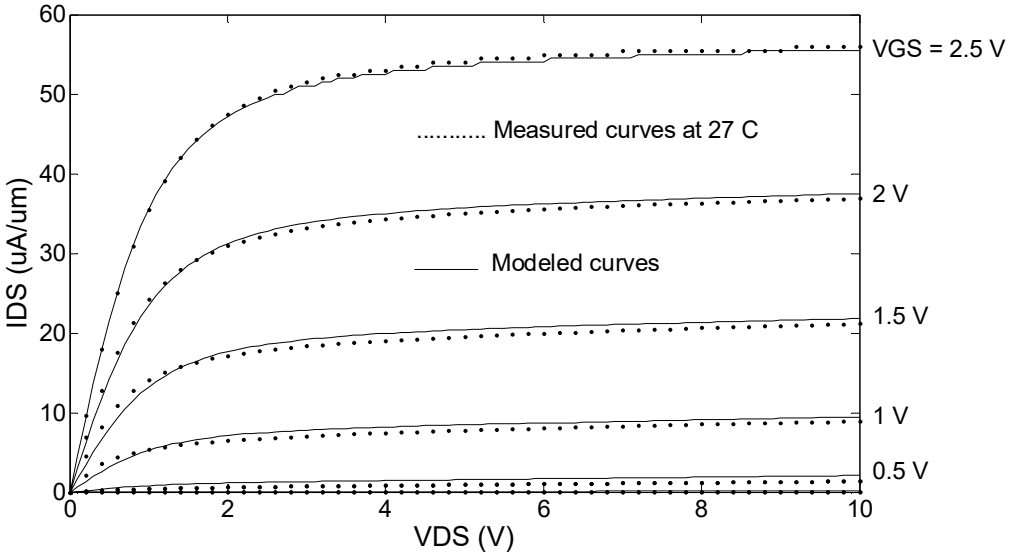


Figure 2.8. Measured and modeled I_{ds} vs. V_{ds} curves of an EM SiC JFET with V_{th} of +0.43 V at 27°C.

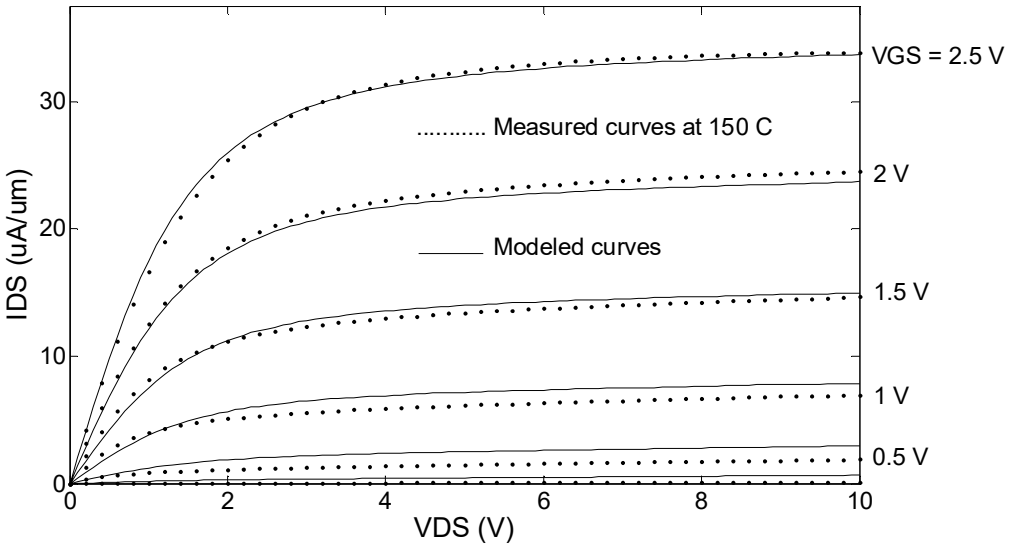


Figure 2.9. Measured and modeled I_{ds} vs. V_{ds} curves of an EM SiC JFET with V_{th} of +0.43 V at 150°C.

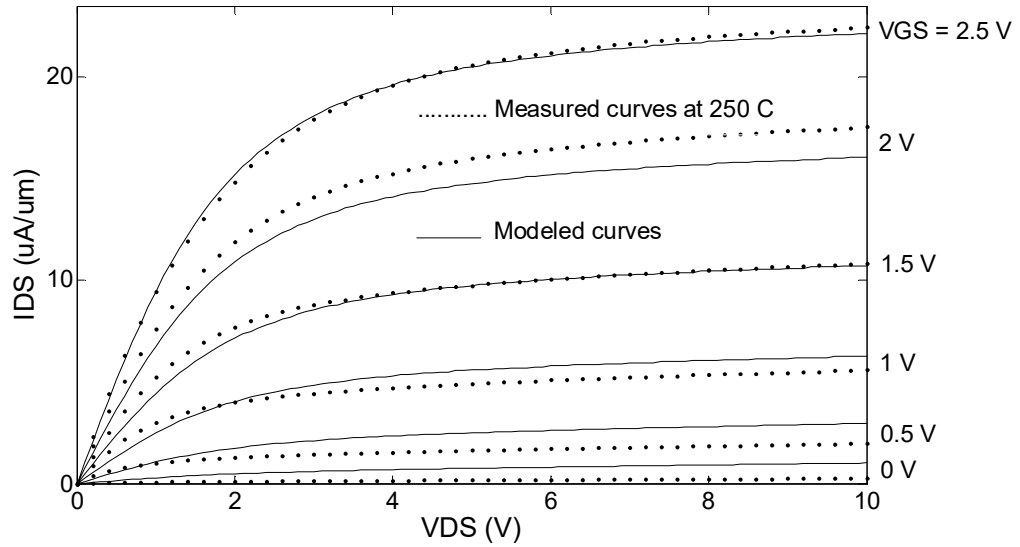


Figure 2.10. Measured and modeled I_{ds} vs. V_{ds} curves of an EM SiC JFET with V_{th} of +0.43 V at 250°C.

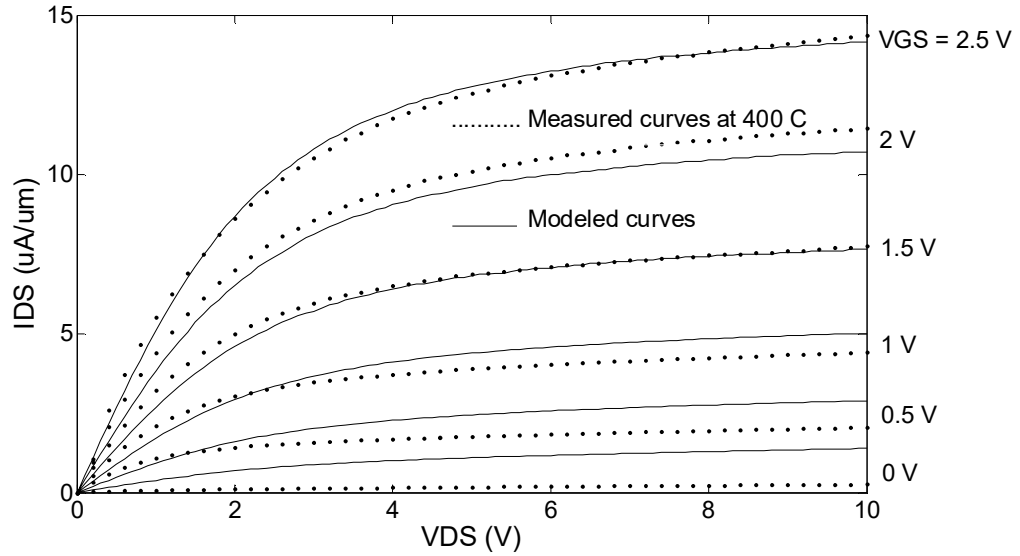


Figure 2.11. Measured and modeled I_{ds} vs. V_{ds} curves of an EM SiC JFET with V_{th} of +0.43 V at 400°C.

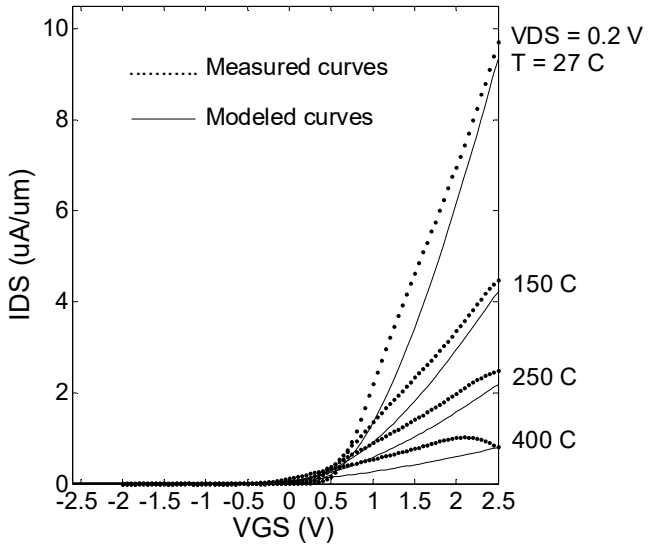


Figure 2.12. Measured and modeled I_{ds} vs. V_{gs} curves of an EM SiC JFET with V_{th} of +0.43 V from 27°C to 400°C.

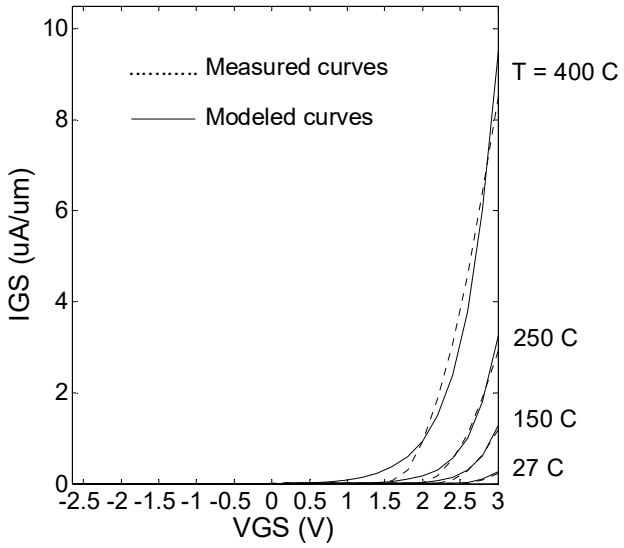


Figure 2.13. Measured and modeled I_{gs} vs. V_{gs} curves of an EM SiC JFET with V_{th} of +0.43 V from 27°C to 400°C.

2.3 Effect of Temperature on SiC JFET over the Range of 25°C to 400°C

Figures 2.14, 2.15, and 2.16 show small signal parameters of transconductance (g_m), output resistance (r_o), and V_{th} of SiC JFET devices change in the temperature range of 25°C to 400°C. The performance reduction is not as great as a comparable to SiC NMOS [14]. In high temperature analog design, all of these variations should be taken into account in order to have a circuit operating in a wide temperature range.

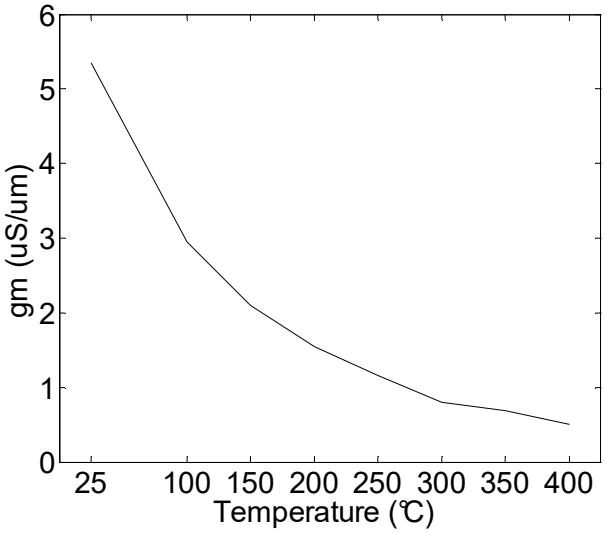


Figure 2.14. Effect of temperature over the range of 25°C to 400°C on g_m is –13 (μS/(μm×°C)).

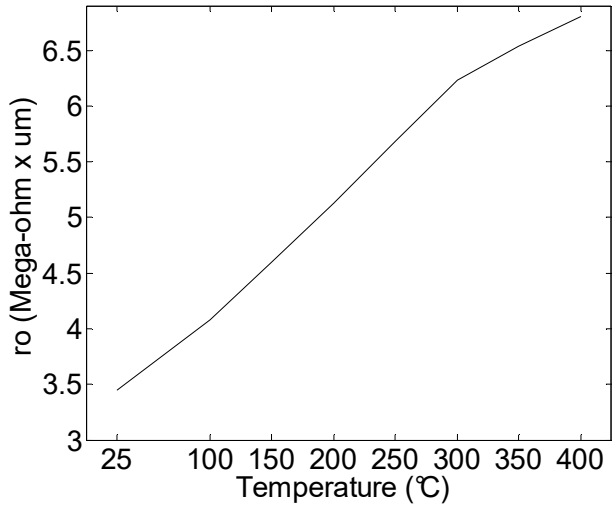


Figure 2.15. Effect of temperature over the range of 25°C to 400°C on r_o is 8.9 ((KΩ × μm)/°C).

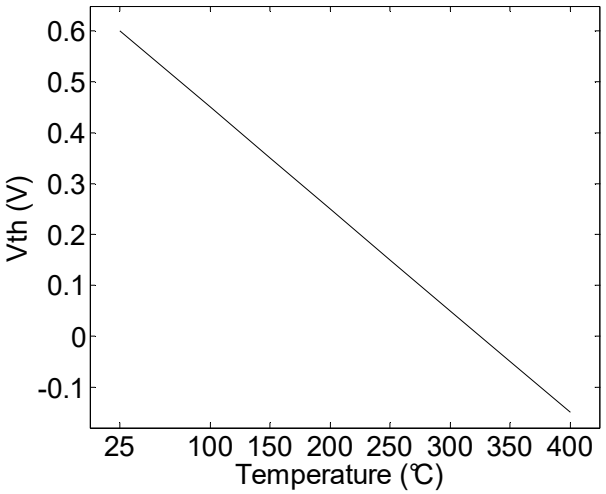


Figure 2.16. Effect of temperature over the range of 25°C to 400°C on V_{th} is –2.2 (mV/°C). V_{th} of the tested device is 0.6 V at 25°C.

CHAPTER III

SILICON CARBIDE JFET BASED ANALOG BLOCKS AND PERFORMANCE ANALYSIS

3.1 Device Characteristics for Design

In order to evaluate the device capabilities for amplification stages, maximum transconductance and average output resistance of a number of EM and DM devices based on their V_{th} are measured and shown in figure 3.1. Figure 3.2 shows a basic self-biased Common Source (CS) amplifier illustrating the driver J1 as an EM JFET and current source or load transistor J2 as a DM JFET. Obviously, driver transistor J1 must have higher V_{th} than J2 to drive the drain current. Moreover, EMs show higher transconductance and output resistance than DMs; therefore, there are advantages using EMs as drivers. Although, EM devices have higher intrinsic gain compare to DMs, but there is a tradeoff between intrinsic gain and GSVR requirement. If higher GSVR is required instead of higher gain, then DMs can also be used as drivers, and the load transistor always has to have lower V_{th} than the driver transistor. As mentioned in chapter two, fabrication restriction on utilizing CL as a design parameter is one of the design challenges that is overcome by using V_{th} instead of CL. For instance, as device V_{th} increases from negative to positive, both output resistance and transconductance increase, which is shown in figure 3.1; therefore, V_{th} can play a similar, but not an exact, role as

CL. The difference between the role of CL and V_{th} is that CL is inversely proportional to the transconductance, where V_{th} is in direct proportion. Increasing CL increases output

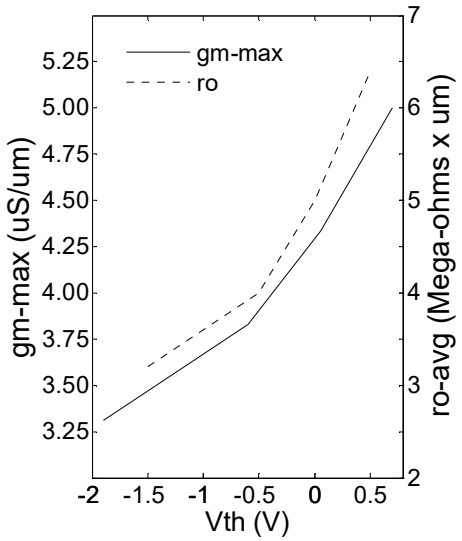


Figure 3.1. Measured maximum transconductance and average output resistance variation of the devices based on their V_{th}.

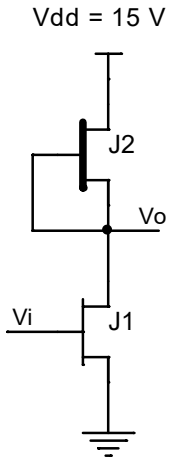


Figure 3.2. Basic self-biased CS amplifier.

resistance, but decreases transconductance, while increasing V_{th} from negative to positive, in these devices, increases both output resistance and transconductance.

To illustrate utilizing V_{th} in the absence of CL for gain adjustment, level one drain current equation (1) can be considered [19]. Equation (2) represents drain current in the saturation region. By applying (2) into the gain relation (3) and knowing that both EM

$$I_D = \beta_1 \cdot (V_{gs} - V_{th1})^2 (1 + \lambda_1 V_{ds}) \cdot \tanh(\alpha \cdot V_{ds}) \tag{1}$$

$$I_{D_{Sat}} = \beta_1 \cdot (V_{gs} - V_{th1})^2 (1 + \lambda_1 V_{ds}) \tag{2}$$

$$A_{v_{CSA}} = -gm \cdot (r_{o1} // r_{o2}) \tag{3}$$

$$A_{v_{CSA}} = -\frac{2\beta_1 \cdot (V_{gs} - V_{th1})(1 + \lambda_1 V_{ds})}{\lambda_1 \cdot \beta_1 \cdot (V_{gs} - V_{th1})^2 + \lambda_2 \cdot \beta_2 \cdot V_{th2}^2}$$

$$Knowing: \ \beta_1 = \beta_2 \ \ \& \ \ (1 + \lambda_1 V_{ds}) \approx 1$$

$$A_{v_{CSA}} = -\frac{2(V_{gs} - V_{th1})}{\lambda_1 \cdot (V_{gs} - V_{th1})^2 + \lambda_2 \cdot V_{th2}^2} \tag{4}$$

$$\frac{\partial A_{v_{CSA}}}{\partial V_{th2}} = \frac{4(V_{gs} - V_{th1}) \cdot \lambda_2 \cdot V_{th2}}{(\lambda_1 \cdot (V_{gs} - V_{th1})^2 + \lambda_2 \cdot V_{th2}^2)^2} = 0$$

$$\lim_{V_{th2} \to 0} A_{v_{CSA}} = -\frac{2(V_{gs} - V_{th1})}{\lambda_1 \cdot (V_{gs} - V_{th1})^2 + \lambda_2 \cdot V_{th2}^2}$$

$$A_{v_{CSA}}(\max) = -\frac{2}{\lambda_1 \cdot (V_{gs} - V_{th1})} \tag{5}$$

and DM have the same dimensions except different FLs, equation (4) is obtained. Equation (5) shows that if V_{th} of J2 tends to zero, maximum gain can be achieved. This means that moving J2's V_{th} closer to J1's causes current and transconductance drop, but the large increase in output resistance results in an increase on the overall gain. It has been realized that in a basic CS amplifier, if V_{th} of J1 and J2 are typically chosen to be +0.5 V and –0.5 V, respectively, high gain with reasonable drain current can be obtained. Since, variation of V_{th} is proportional to overall gain, its effect is sometimes undesirable, i.e., when variation of V_{th} is due to fabrication process variation. In order to illustrate how much this variation will affect the overall gain, a number of CS amplifiers with driver and load transistors having various V_{th}s is tested, and the result is shown in figure 3.3. The peak point is 41 –V/V, and the minimum is 24 –V/V. Equation (4) can also be used to calculate this result.

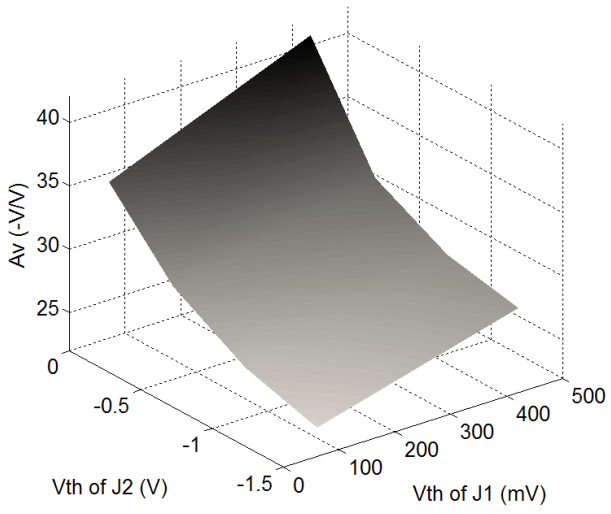


Figure 3.3. Gain variation of a CS amplifier based on the V_{th} variation of the driver and current source load transistors.

Process variation in the form of V_{th} variation can be compensated by using a number of circuit techniques, such as in [20]. Because the design and fabrication of SiC JFET-based circuits are in the early stage, the aim of this research is to avoid complexity and employ a minimum number of transistors; therefore, this technique will only be addressed without using it. Another design parameter is CW. CW can be used as a current adjusting parameter with no fabrication restrictions throughout the design.

3.2 Compensation of Threshold Voltage Variation

A compensation technique [20] for process variation in the form of V_{th} variation is shown in figure 3.4. Nodes A, B, and C are in the same voltage level, since the area of

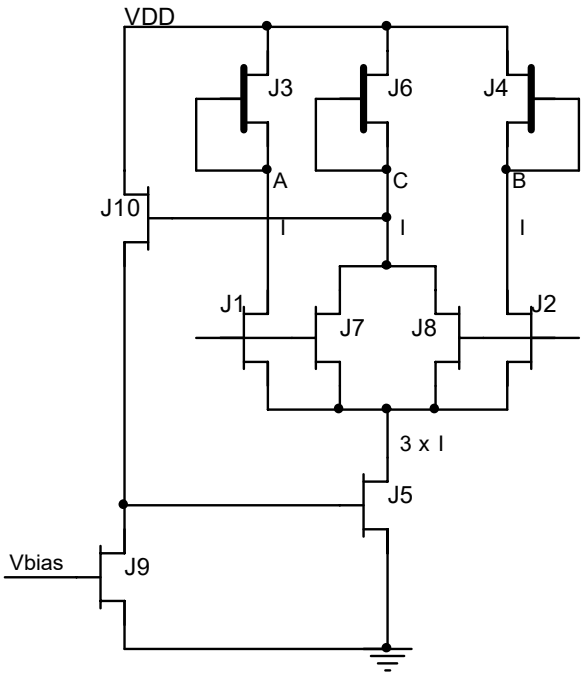


Figure 3.4. A compensation technique for process variation in the form of V_{th} variation.

J7 and J8 are half the areas of J1 and J2. A negative feedback loop through node C, J10, J5, and again node C corrects the amount of the EM devices (J1 and J2) currents to keep the quiescent voltage of V_Q unchanged. Figure 3.5 illustrates a condition when DM mode devices (J3 and J4) are above or below their nominal V_{th}. In this case, negative feedback

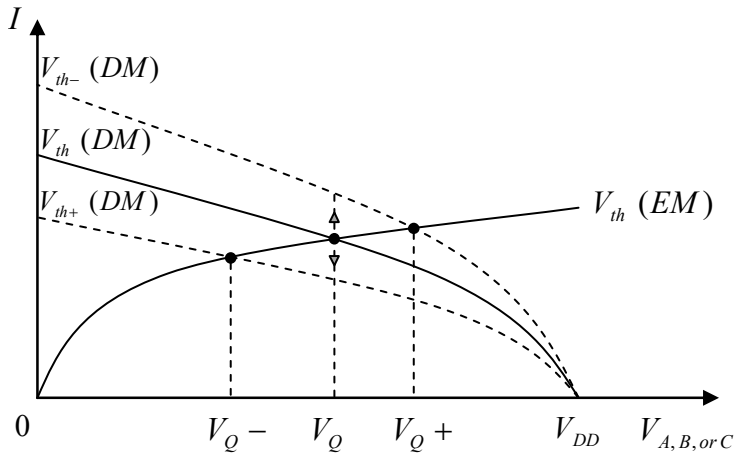


Figure 3.5. Compensating V_{th} variation of DM JFETs (J3 and J4) by adjusting EM JFETs (J1 and J2) currents.

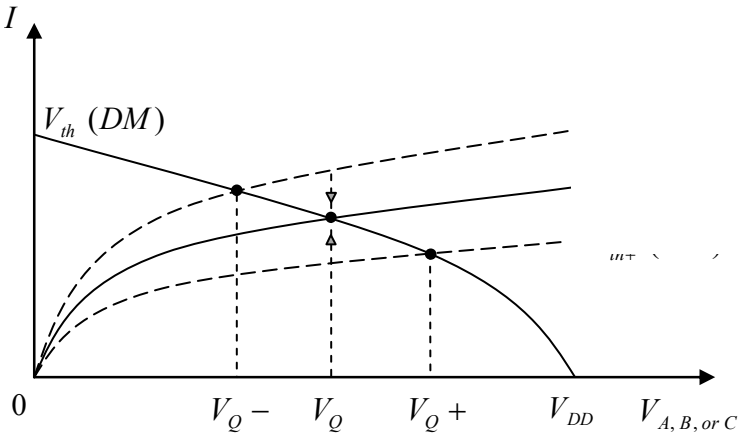


Figure 3.6. Compensating V_{th} variation of EM JFETs (J1 and J2) by adjusting the same JFETs currents.

results in increase or decrease of the EM devices currents to keep V_Q unchanged. In a condition that the EM devices V_{th} is above or below their nominal value in figure 3.6, the loop decreases or increases the EM devices currents, respectively. This technique could be one of the solutions for compensating process variation in the form of V_{th} variation.

3.3 Current Source Configurations and Characteristics

DM devices are used as current sources or loads for amplifiers. Figures 3.7(a) to (f) show various load configurations in self-biased and current source mode. Self-biasing

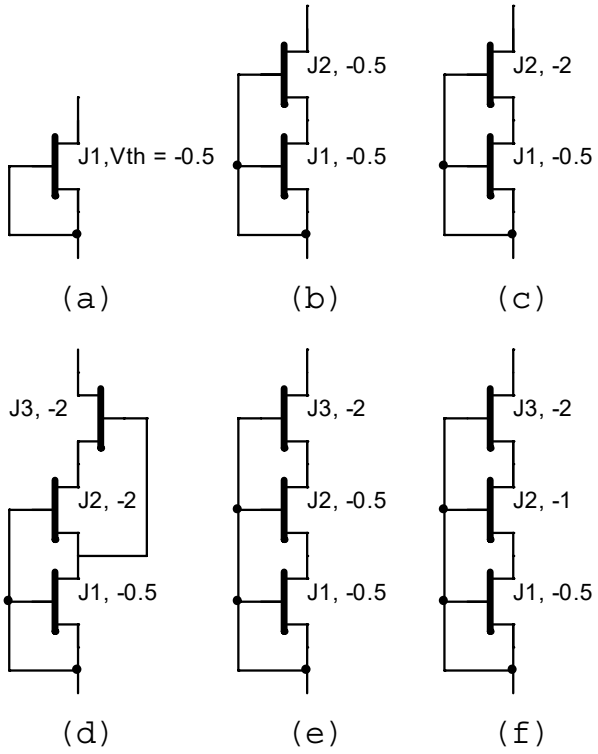
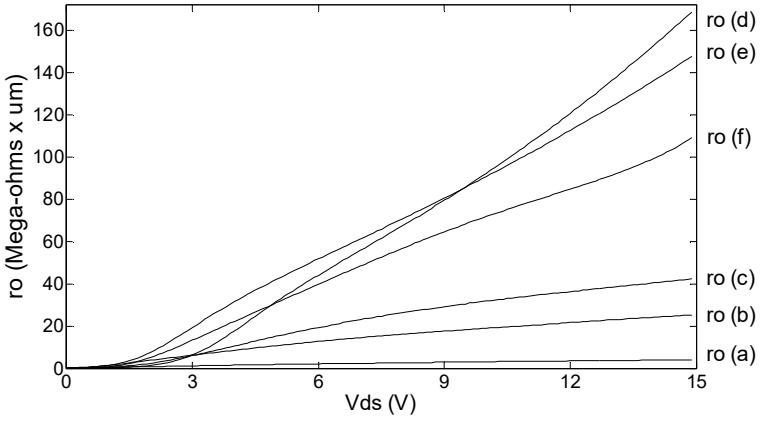
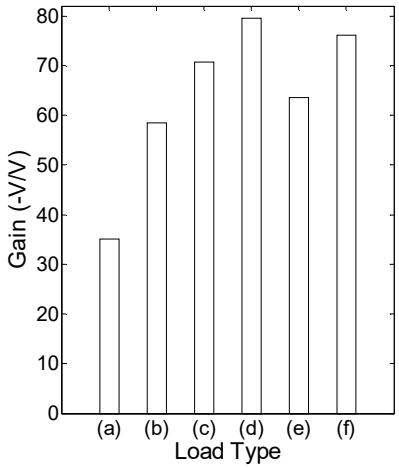


Figure 3.7. (a) DM SiC JFET based current source or load in self-biased configuration. (b)-(f) Cascoded loads for higher output resistance.

eliminates additional biasing circuits. The corresponding output resistance profile of each load configuration is measured and presented in figure 3.8(a). The single transistor load in figure 3.7(a) has the least output resistance, while double transistors with cascoded



(a)



(b)

Figure 3.8. (a) Measured output resistance curves of DM SiC JFET loads in various (a) to (f) configurations. (b) Measured gain of CS amplifiers with various load types from (a) to (f).

configurations show quite an improvement. In figure 3.7(b), two exact devices with the same V_{th} are used. However, if J2 with a more negative V_{th} is used (figure 3.7(c)), the result is more current deliverability at the same time higher output resistance. In other words, J1 will be able to maintain more drain to source voltage (as long as J2 is on) moving more towards saturation region and benefiting from its higher output resistance. When such configuration is used in the basic CS amplifier of figure 3.2, higher output resistance, along with higher current deliverability enables the driver to maintain higher transconductance, resulting in a gain improvement, as shown in figure 3.8(b). Equations (6) through (9) show the overall output resistance of each configuration with respect to

$$r_{o(a)} = r_{o1} \tag{6}$$

$$r_{o(b,c)} = r_{o1} + r_{o2} + g_{m2} r_{o1} r_{o2} \tag{7}$$

$$r_{o(d)} = r_{o1} + r_{o2} + r_{o3} + g_{m2} r_{o1} r_{o2} + g_{m2} g_{m3} r_{o1} r_{o2} r_{o3} + g_{m3} r_{o3} r_{o2} \tag{8}$$

$$r_{o(e,f)} = r_{o1} + r_{o2} + r_{o3} + g_{m2} r_{o1} r_{o2} + g_{m2} g_{m3} r_{o1} r_{o2} r_{o3} + g_{m3} r_{o3} (r_{o1} + r_{o2}) \tag{9}$$

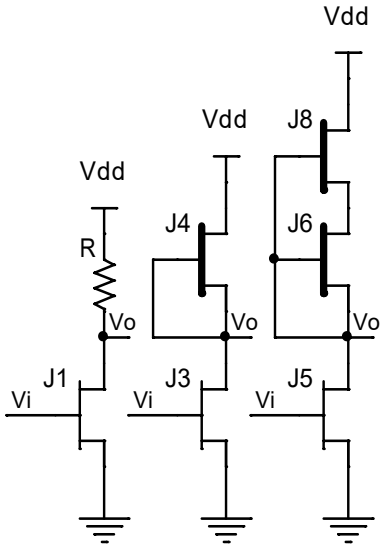
the transconductance and output resistance of the transistors. As the number of cascoded transistors increases in figures 3.7(d) [21] to 3.7(f), higher output resistance can be observed. Figure 3.7(e) shows a better curve in lower V_{ds} compared to others, but less current deliverability, resulting in lower gain, shown in figure 3.8(b). Figure 3.7(f) is an improved version of figure 3.7(e), where the amount of current can be determined by V_{th}

of J2 and J3. Based on the current or gain requirements of a CS amplifier, a load configuration among figures 3.7(a) to (f) can be chosen using figures 3.8(a) and (b).

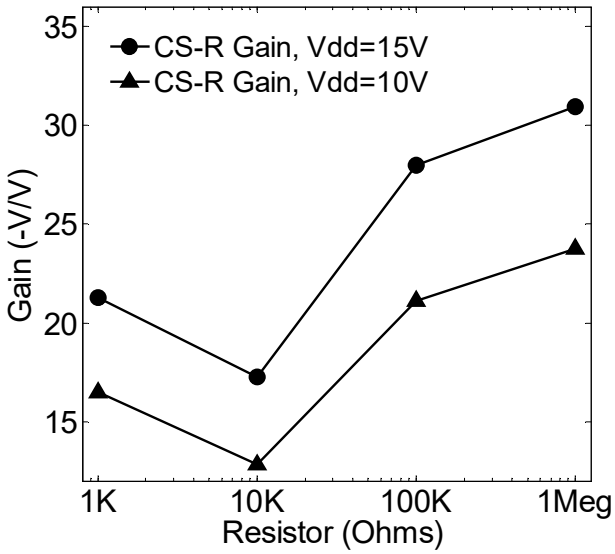
3.4 Gain and Small Signal Analysis of CS Amplifier

As mentioned earlier, V_{th} of a SiC JFET is a significant parameter in determining the performance of the SiC JFET-based analog circuits. In order to analyze the gain performance, three types of CS amplifiers are constructed. Respectively, figures 3.9(a), (b), and (c) show CS with resistive load (CS-R), CS with active load or DM transistor (CS-A) in self-biased configuration, and CS with a cascoded DM load (CS-Cas) in self-biased configuration. Transistors J1, J3, and J5 are EM, and J4, J6, and J8 are DM devices. Since EM devices exhibit lower output conductance (g_d) and higher transconductance (g_m) than DM mode devices, therefore, they are better suited to be the drivers. Figures 3.9(d) and 3.10 show the measured gain for these three configurations. The CS-Cas configuration where the load transistors V_{th}s are –0.5 V produces the highest gain of 49.8 when V_{dd} = 10 V and 67.2 when V_{dd} = 15 V. Figures 3.11(a) and (b) analyze and reveal the quantities of the driver g_m, driver output conductance (g_{dD}), and load output conductance (g_{dL}) where they set the gain points of figure 3.10. To be more specific, when the V_{th} of the load transistor is –0.5 V in CS-Cas, driver g_m = 12.4 µS/µm, driver g_d is g_{dD} = 120 nS/µm, and load g_d is g_{dL} = 64.5 nS/µm, then the DC or low frequency gain equation (10) is at the highest point of:

$$| Gain_{LF,CS-Cas} | = | \frac{-gm}{gd_D + gd_L} | = 67.2 V/V \qquad (10)$$



(a) (b) (c)



(d)

Figure 3.9. (a) CS-R. (b) CS-A. (c) CS-Cas. (d) Measured gain of CS-R in 1 KΩ to 1 MΩ load resistor range for two V_{dd} of 10 V & 15 V.

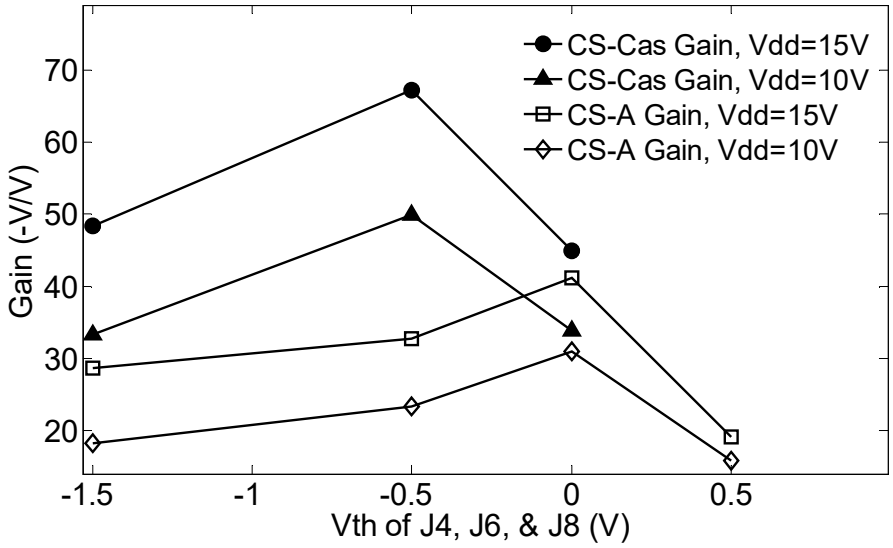
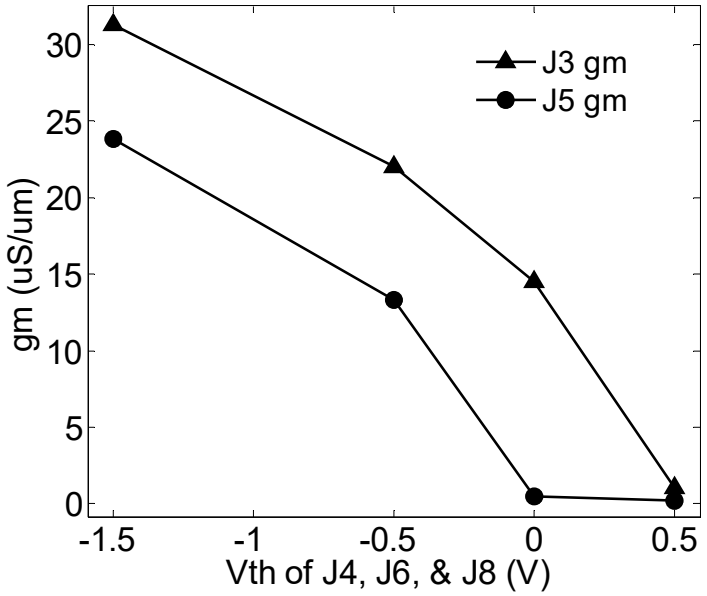
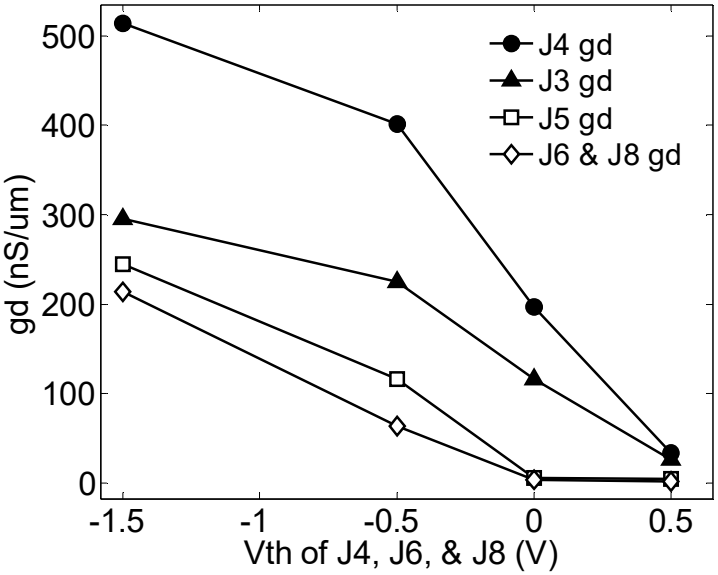


Figure 3.10. Measured gain of CS-A and CS-Cas in load transistor V_{th} range of –1.5 V to +0.5 V for two V_{dd} of 10 V & 15 V. Because the transistors have relatively high g_d, gain increase is high and noticeable, when V_{dd} increases.

Using the extracted SPICE model from modeled curves, CS-Cas amplifier is simulated, and the gain is 62.8 –V/V. Part of the deviation between the measured and simulated results comes from the procedure of modeling and another part from the overall characterization and modeling error, where $g_m = \partial I_{ds} / \partial V_{gs}$ of the modeled curves at the lower V_{ds} voltages are less than the g_m of the actual measurement. In the modeling process, parameters such as output conductance of the transistors are modeled slightly higher than their actual values so that the circuit simulation result does not overestimate the test result.



(a)



(b)

Figure 3.11. (a) g_m characteristics of J3 and J5 transistors and (b) g_d characteristics of J4, J6, and J8 transistors versus V_{th} of the load transistors that resulted the gain points of CS-A and CS-Cas in figure 3.10, when V_{dd} is 15 V. CL and CW of the devices are 2 μm and 2 mm.

3.5 Frequency Response of the CS-Cas

The frequency and phase response of the CS-Cas amplifier in no load condition is measured and reported in figure 3.12. The cutoff frequency of the amplifier is 880 kHz, and the gain bandwidth product is 58 MHz. The frequency response can be improved significantly by making the devices smaller. These devices are fabricated for high current and power electronics applications and their CW is large. Dramatic improvement may not be feasible, since the gate to drain area or the gate to drain capacitance is larger than the gate to source capacitance, as shown in figure 2.1 in the previous chapter. In other words, in the gain equation (11), the Miller effect of the driver transistor becomes the significant limiting factor of the frequency response at higher frequencies when low frequency gain is too high, gate to drain capacitance is too large, or both. The ω_H parameter decreases,

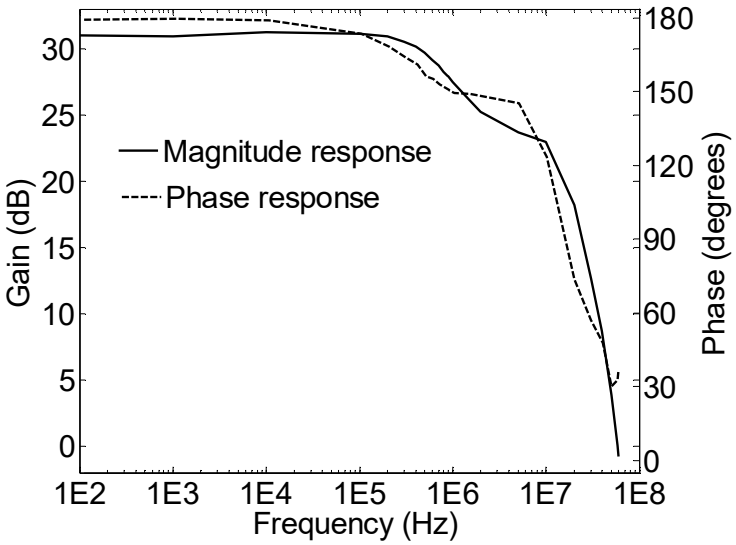


Figure 3.12. Magnitude and phase response of the CS-Cas configuration. Cutoff frequency is 880 kHz and gain bandwidth product is 58 MHz.

thus the overall gain decreases.

$$Gain_{CS-Cas}(\omega) = \frac{Gain_{LF,CS-Cas}}{1 + j\frac{\omega}{\omega_H}} = \frac{\frac{-gm}{gd_D + gd_L}}{1 + j\frac{\omega}{1 \Big/ (R_{Supply}Cgs + R_{Supply}Cgd(1 + |\frac{-gm}{gd_D + gd_L}|) + \frac{Cds}{gd_D + gd_L})}} \quad (11)$$

3.6 Switching Characteristics of the CS-Cas

Switching characteristics of the CS-Cas such as falling propagation delay ($t_{pf} = 10.2ns$), rising propagation delay ($t_{pr} = 19.8ns$), output fall time ($t_f = 10ns$), and output rise time ($t_r = 47.2ns$) are measured in no load condition and are shown in figure 3.13. The measurement reveals that the switching function of the amplifier at the highest

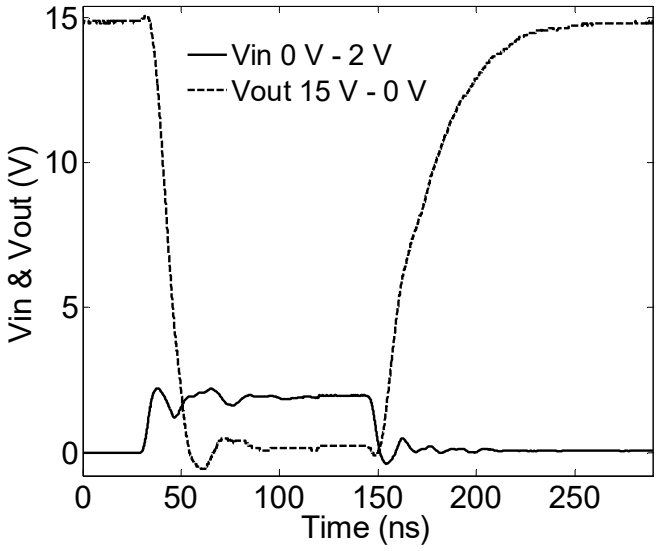


Figure 3.13. Switching characteristics of the CS-Cas configuration.

gain point of 67.2 –V/V, given an input with 50% duty cycle, is limited to 10 MHz. If the DC gain is decreased, the Miller effect will be reduced, and the switching frequency will be increased.

3.7 Differential Amplifier and Gain Analysis

Two types of diffamps are presented. They both utilize cascoded DM loads of figure 3.7(b) to enhance the gain. Figure 3.14 is a basic type of diffamp with J1 to J4 as EM devices (V_{th}s are +0.5 V) and J5 to J8 as DM devices (V_{th}s are –0.5 V). Measured transfer curves of figure 3.14 are presented in figure 3.15 showing gain of –22 V/V on each output. This figure reveals a large amount of offset voltage over 100 mV resulting from the devices mismatches. Chapter four discusses this diffamp in more detail.

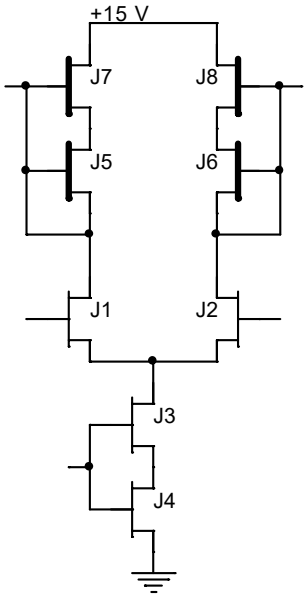


Figure 3.14. Realization of a basic diffamp with cascoded loads.

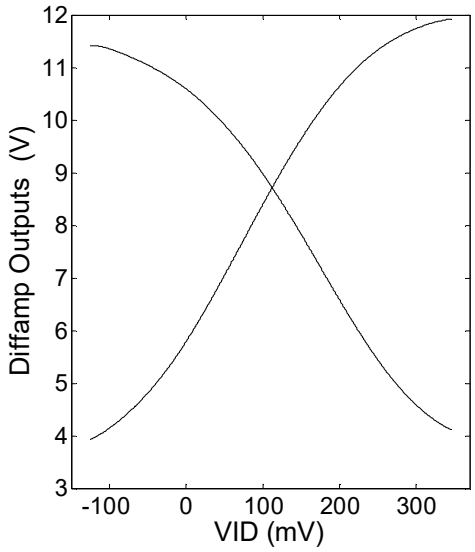


Figure 3.15. Measured transfer curves of the basic diffamp with cascoded loads. Differential gain is –22 V/V on each output.

Another type of diffamp is presented in figure 3.16 that consists of a Common Gate (CG) amplifier along with cascoded loads. The addition of a CG amplifier stage significantly improves the gain performance, where the measured transfer curve of figure 3.17 shows gain of –98.6 V/V on each one of the outputs. A large amount of offset associated with this diffamp can also be observed in figure 3.17. It should be mentioned that there is a tradeoff between the GSVR requirement of J5 and J6 and output voltage swing; therefore, whenever both high voltage gain and high output voltage swing are required, this type of diffamp will not be an ideal configuration.

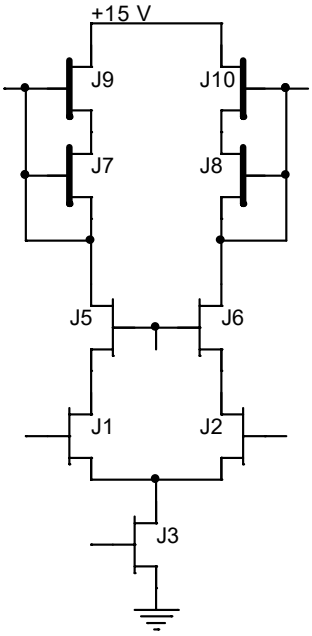


Figure 3.16. Diffamp with cascoded loads along with CG amplifier.

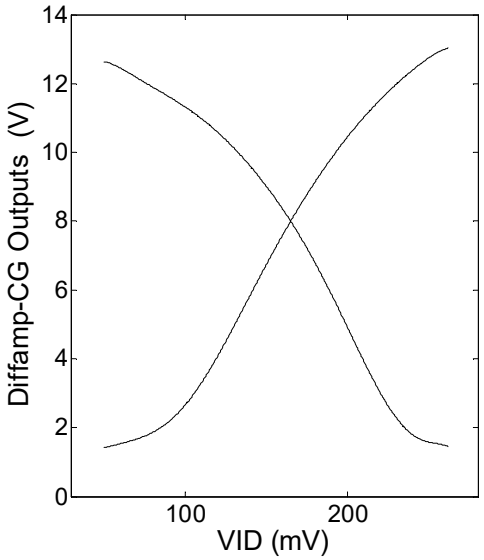
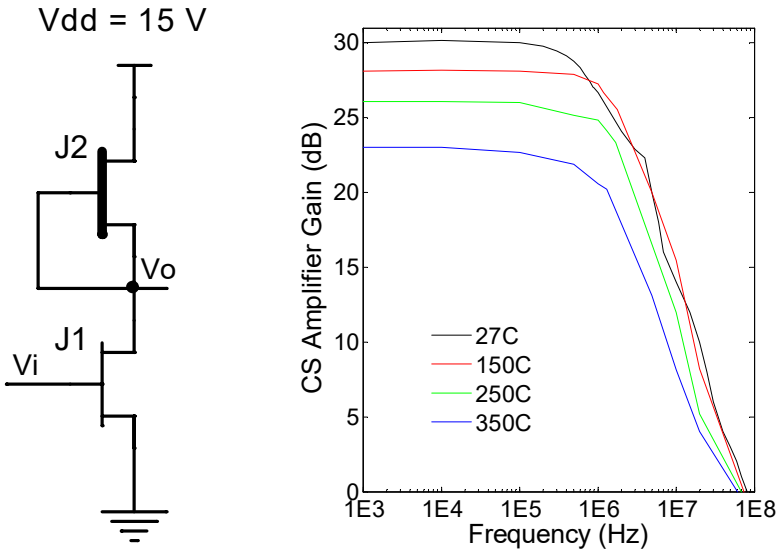


Figure 3.17. Measured transfer curves of the diffamp with CG amplifier. Differential gain is –98.6 V/V on each output.

3.8 Effect of Temperature on Common Source Amplifier

The final section of this chapter experiments with temperature effect on a CS amplifier with an EM driver of J1 (V_{th} = 0.5 V) and a DM current source of J2 (V_{th} = –0.5 V), shown in figure 3.18(a). This section quickly overviews the characteristics of a SiC JFET-based CS amplifier over a range of temperature variation. Obviously, more comprehensive and experimental work can be pursued on amplification stages at elevated temperature that may utilize this section as a starting point. The main objective of this dissertation is to identify the shortcomings at room temperature and to provide solutions, but at the same time, it is important to keep current work connected to the future work, which might emphasize on high temperature design.



(a) (b)

Figure 3.18. (a) SiC JFET based CS amplifier with an EM driver J1 and a DM current source J2. (b) Effect of temperature over the range of 27°C to 350°C on frequency response of the CS amplifier is measured.

In figures 3.18(b) and 3.19, both AC and DC characteristics of the CS amplifier are measured and presented. Measurement shows that both gain and bandwidth decrease as temperature increases from 27°C to 350°C. The rate of the temperature variation effect within the range of 27°Cto 150°C is slightly less than the range of 150°C to 350°C on frequency response. In figure 3.19, the measured transfer characteristics of the CS amplifier shows a gain performance drop from –37.7 V/V to –18 V/V over the 27°C to 350°C range. Such gain drop is a direct result of intrinsic gain decrease when temperature increases. As a matter of fact, the large transconductance reduction (although output resistance increases) shown in figure 2.14 of chapter two can justify the intrinsic gain

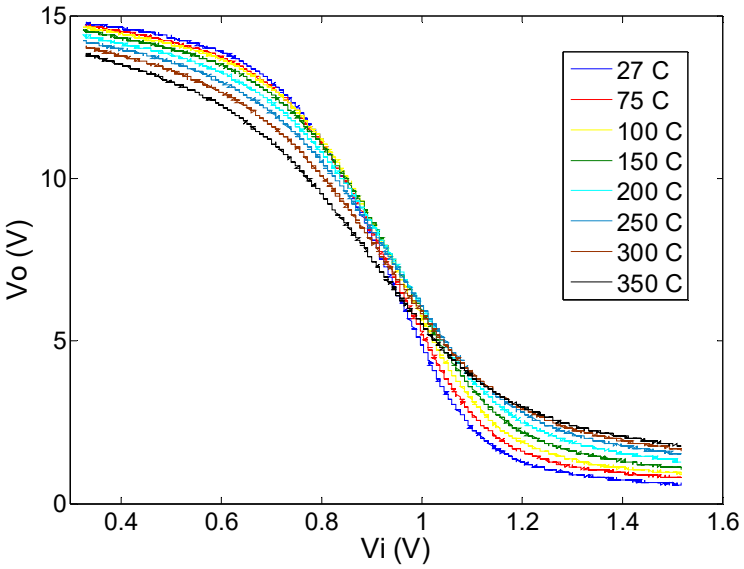


Figure 3.19. Effect of temperature over the range of 27°C to 350°C on transfer function of the SiC JFET based CS amplifier is measured. Gain performance is dropped from –37.7 V/V to –18 V/V over the temperature variation.

drop. Therefore, this is one of the design challenges in DC domain for high temperature opamp design. This needs to be taken into the design considerations and be possibly compensated by taking advantage of appropriate design techniques.

CHAPTER IV

SILICON CARBIDE JFET-BASED OPERATIONAL AMPLIFIER

DESIGN FOR GAIN AND CMRR PERFORMANCE

4.1 Introduction

Although SiC JFETs are superior candidates for high temperature and harsh environment applications, they exhibit significant design challenges even at room temperature, such as low intrinsic gain and low GSVR requirement. The primary goal of this chapter is to design and present an opportunity demonstrating the feasibility of a fully SiC JFET-based opamp. Considering the wide bandgap property of SiC material, the same design is not feasible using silicon JFETs. An opamp based on two types of EM and DM SiC JFETs is designed, fabricated, and tested. In order to offset the low intrinsic gain effect of the transistors and achieve high overall gain and CMRR, gain-enhancing design techniques, such as cascoding and bootstrapping, are applied in a way that the low GSVR requirement is taken into account. The performance of the final opamp shows 67 dB of open loop gain and 73 dB of CMRR. At the end of this chapter, the final opamp is evaluated for high temperature application, and an immediate shortcoming of the gain reduction in the DC domain is discussed.

4.2 Circuit Configuration and Description:

The overall configuration of the opamp is shown in figure 4.1. It consists of two types of diffamps, Level Shifters (LSs), and a Source Follower (SF). The lead compensation scheme with external Compensation Elements (CEs) of CE1 and CE2 can be seen in the outputs of the diffamp1. Diffamp2 sets the overall gain of the opamp and converts differential input to single-ended output. The main purpose of this overall structure is to achieve high gain and CMRR while considering the low GSVR requirement. The final opamp is capable to drive 1 nF capacitive load.

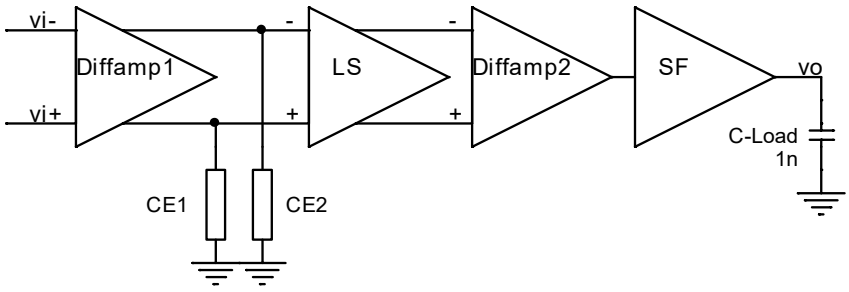


Figure 4.1. The overall configuration of the designed opamp with external CEs of CE1 and CE2.

4.2.1 Differential Amplifier with Cascoded Load

Input stage, diffamp1, shown in figure 4.2, includes four EM SiC JFETs, J1 through J4, and four DM transistors, J5 through J8, with V_{th} of +0.5 V and –0.5 V, respectively. In analog design based on these SiC JFETs, the V_{th} parameter is a great asset to determining the performance of the circuits. In other words, V_{th} plays a similar role as CL does in CMOS-based design. In fact, the fabrication of SiC JFETs with

various CLs all on the same die is a very complicated task because the channel is vertical; therefore, V_{th} is used as a design parameter. Tail transistors, J3 and J4, are also EMs in

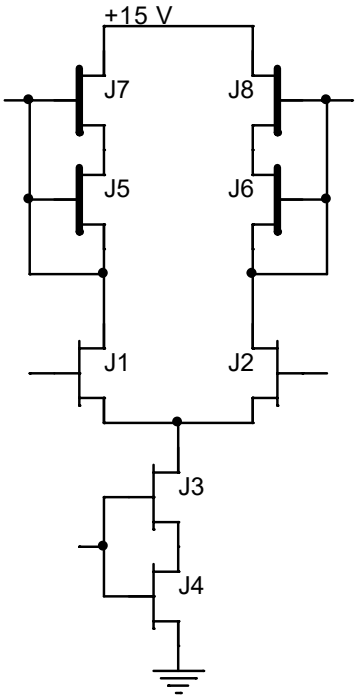


Figure 4.2. Input stage, diffamp1, with self biased cascoded loads.

order to have higher CMRR. A disadvantage of using EM devices as input drivers is their lower GSVR, which makes the Input Common Mode Range (ICMR) of the opamp limited. On each side of the diffamp1 outputs, two DM load transistors are located in self-biased and cascoded configuration, eliminating any additional biasing circuit and improving the output resistance of the current source load. The measured transfer curves of figure 4.3 shows a gain of –22 V/V on each output. It is noticeable from figure 4.3 that there is a large amount of offset voltage (112 mV) associated with diffamp1, due to

drivers and load transistors mismatches. The fabrication technology for SiC devices and, more specifically, SiC JFETs is still growing and until the perfection of the fabrication process, device imperfections will reveal such issues. Small signal differential gains of the diffamp1 for each output are also calculated and shown in equations (1) and (2).

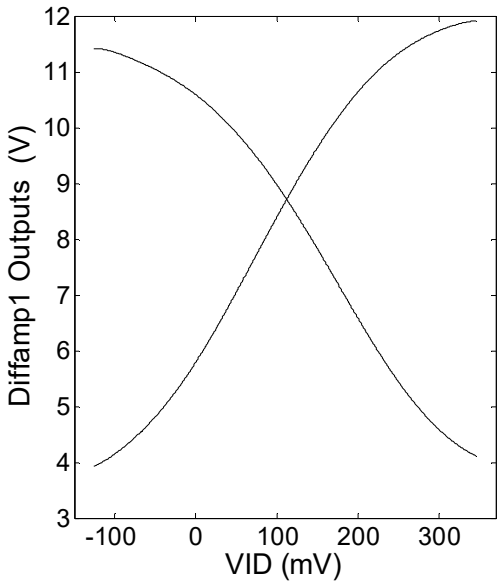


Figure 4.3. Measured transfer curves of the diffamp1 with gain of –22 V/V.

$$A_{v_1} = \frac{v_{d1}}{v_{g1} - v_{g2}} = \frac{-g_{m1} r_{o1} (r_{o5} + r_{o7} + g_{m7} r_{o5} r_{o7})}{2(r_{o1} + r_{o5} + r_{o7} + g_{m7} r_{o5} r_{o7})} \quad (1)$$

$$A_{v_2} = \frac{v_{d2}}{v_{g1} - v_{g2}} = \frac{g_{m2} r_{o2} (r_{o6} + r_{o8} + g_{m8} r_{o6} r_{o8})}{2(r_{o2} + r_{o6} + r_{o8} + g_{m8} r_{o6} r_{o8})} \quad (2)$$

In figure 4.4, the frequency response of the diffamp1 measures a cutoff frequency of 620 kHz and a unity gain frequency of 20.5 MHz. These devices are designed and fabricated for high current and power electronics applications, which their gate to drain and gate to source junction areas are very large, so are their associated parasitic capacitances. By inspecting the device structure, it can be seen that the area between gate to drain is even larger than the area between gate to source. This, plus size of the devices can explain the limitations seen in the measured bandwidth.

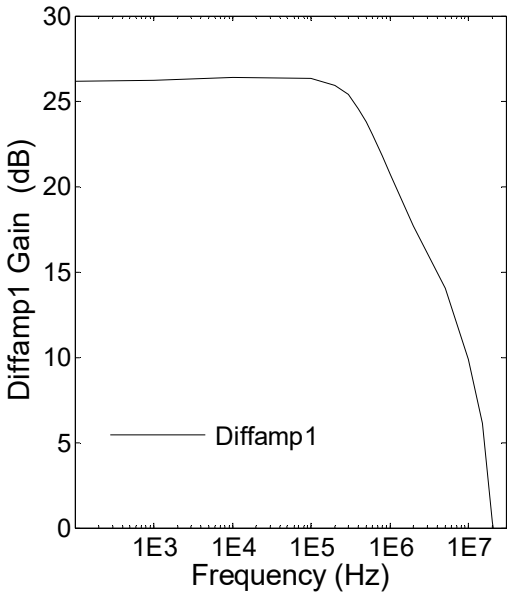


Figure 4.4. Measured frequency response of the diffamp1.

4.2.2 Level Shifters

Diffamp1 is followed by LSs, shown in figure 4.5. LSs are source followers containing two diode connected EM devices on each side, J19 to J22, biasing diffamp2

and delivering signals to it. In order not to overdrive the diffamp2, the number of the diode connected devices can be determined based on the GSVR requirements of the diffamp2's input devices. Transistors J9 and J10 are in self-biased configuration acting as current sources.

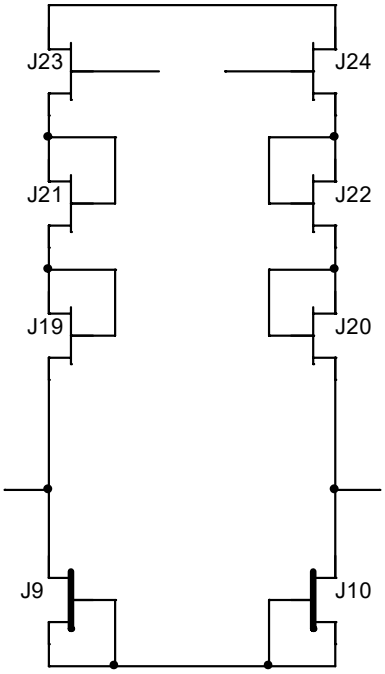


Figure 4.5. LSs with diode connected EM devices.

4.2.3 Gain Enhanced Differential Amplifier and Convertor

The second gain stage of the opamp, diffamp2, in figure 4.6, containing four EM transistors, J11 through J14, and four DMs, J15 through J18, is a compact high gain stage with differential to single ended capability. The reason for using a high gain diffamp in the second stage instead of using a high gain CS amplifier is to improve the CMRR

performance and, most importantly, to meet the low GSVR requirement where a high gain CS amplifier can violate it. The function of the diffamp2 requires explanation

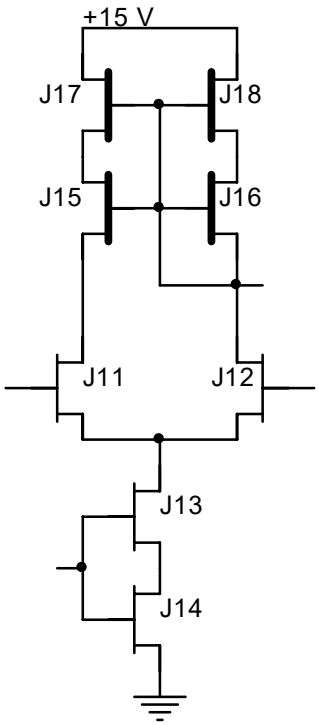


Figure 4.6. Gain enhanced bootstrapped diffamp2 and differential to single ended convertor

because it uses a bootstrapping technique [22] and a controlled positive feedback to enhance the gain performance of the amplifier. The combination of J15 and J17 transistors creates a source follower configuration that forces the drain voltage of J11 to change in the same direction as the drain of J12. Cascoded J16 and J18 transistors are in self-biased configuration and act as a current source. Any positive and differential input applied to the gate of J11 is amplified in the drain of J12 in a positive direction. Almost

the same voltage appears at the drain of J11 through the source follower action. This voltage forces current to flow through output resistance of the J11. Since the created currents due to input signal change are almost equal in the source of both J11 and J12, zero current flows through J13 and J14. This causes common mode voltage at the drain of J13 to undergo a large voltage swing to make currents coming from output resistances of J11 and J12 to circulate to J11 and J12 as transconductance currents. If the source follower gain is unity, which is the negative part in the denominator of equation (3) [22], then common mode swing would be infinity. Since it is less than unity, the swing is large, and the overall gain of the diffamp2 is enhanced. Equation (3) shows that the effect of J11 intrinsic gain is reduced by a number in the denominator that is less than unity. In other words, the overall gain of the diffamp2 is improved, which is confirmed by

$$\frac{vd_{11}}{vg_{11}-vg_{12}}=\frac{vd_{12}}{vg_{11}-vg_{12}}= \frac{g_{m11}r_{o11}}{\dfrac{1+g_{m11}r_{o11}}{1+g_{m12}r_{o12}}-\dfrac{g_{m15}r_{o15}+g_{m17}r_{o17}+g_{m15}g_{m17}r_{o15}r_{o17}}{1+g_{m15}r_{o15}+g_{m17}r_{o17}+g_{m15}g_{m17}r_{o15}r_{o17}+\dfrac{g_{m17}r_{o15}r_{o17}}{r_{o11}}\left[1+\dfrac{1}{r_{o15}}+\dfrac{1}{r_{o17}}\right]}} \tag{3}$$

measuring the gain from the transfer curve of figure 4.7. The measured gain is +92 V/V that is more than four times the gain of the diffamp1. Figure 4.7 also shows the offset voltage of 98 mV created by devices mismatches. The frequency response of the diffamp2 in figure 4.8 shows a cutoff frequency of 360 kHz and a unity gain frequency of 19 MHz. Comparing cutoff frequencies of diffamp1 to diffamp2, it is realized that the gain of diffamp2 is increased at the expense of reduced bandwidth.

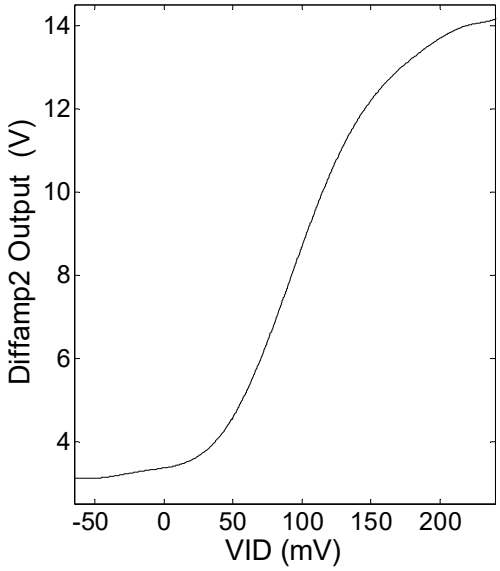


Figure 4.7. Measured transfer curve of the diffamp2 with gain of 92 V/V.

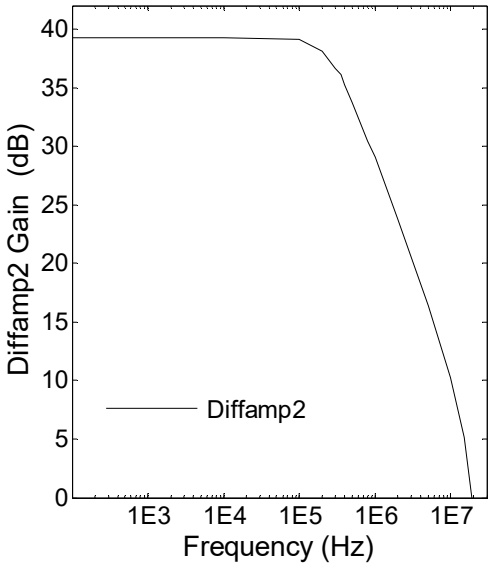


Figure 4.8. Measured frequency response of the diffamp2.

4.2.4 Source Follower

The last stage of the opamp is an SF shown in figures 4.1 and 4.9 capable of driving 1 nF of capacitive load and supplying 60 mA current. Obviously, SF can be redesigned for higher load current capability, if it is needed. Transistor J29 is a DM with V_{th} of –1.5 V in a self-biased configuration as a current source.

4.3 Complete Amplifier

The completed opamp shown in figure 4.9 contains all the described four stages plus a bias stage to set the bias currents of the diffamps. The final design is fabricated and tested, and the performance parameters are shown in figures 4.6 and 4.7 and table 4.1. All of the EM and DM transistors have V_{th} of +0.5 V and –0.5 V, respectively, except

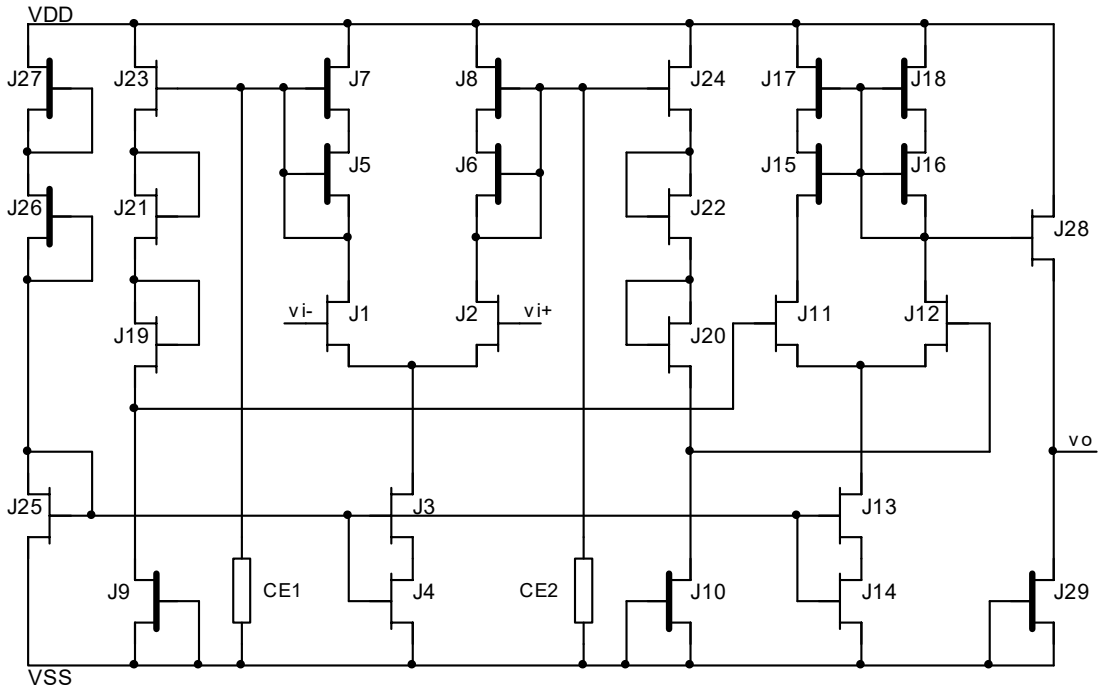


Figure 4.9. Complete schematic of the opamp.

J29 (–1.5 V). Since the fabrication of SiC JFET based circuits is in the early stage, this opamp is fabricated by integrating 29 dies on an aluminum nitride substrate and wire bonding the connections. Each die is 650 μm by 650 μm containing four transistors where only one transistor is used from each die; therefore, large mismatches and offsets are expected. The test result shows that the goal of the SiC JFET-based opamp for high gain and CMRR performance is achieved. It should be mentioned that J1 and J2 are the most vulnerable transistors because they are not protected, and constant high GSVR can cause device overheating, reducing their functional lifetime. Transistors J11 and J12 can also receive high GSVR if they are not appropriately biased. Although EM transistors are desirable for input stages, their drawback is their low GSVR requirement. In case a higher ICMR is desired, the opamp can be redesigned using full DM transistors. The tradeoff of using our DM transistors instead of EMs are lower gain and lower CMRR performance. Figure 4.9 also shows lead compensation scheme at the outputs of the first stage. Outputs of the diffamp1 are grounded by external CE1 and CE2. Both CE1 and CE2 contain Compensation Capacitors (CC) followed by nulling Resistors (RZ) in series. While CCs move the opmap's pole, reducing and controlling the bandwidth, RZs control the right half plane zero of the opamp to introduce phase margin. CCs are 12 nF, and RZs are 20 Ohms.

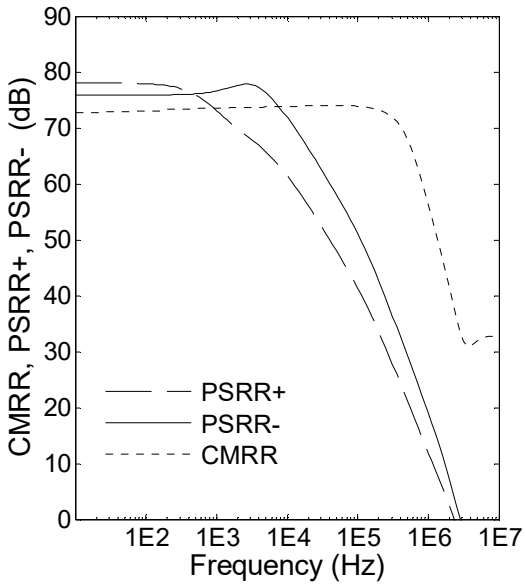


Figure 4.10. CMRR, PSRR+ (dashed line), and PSRR- performance of the opamp.

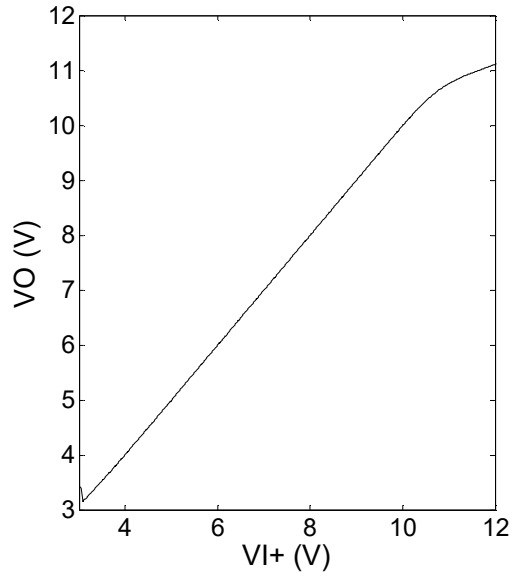


Figure 4.11. ICMR performance of the opamp.

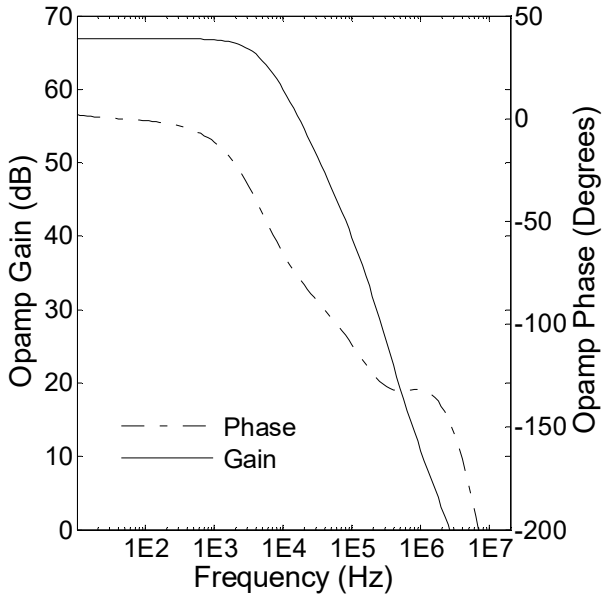


Figure 4.12. Frequency and phase (dashed line) response of the opamp.

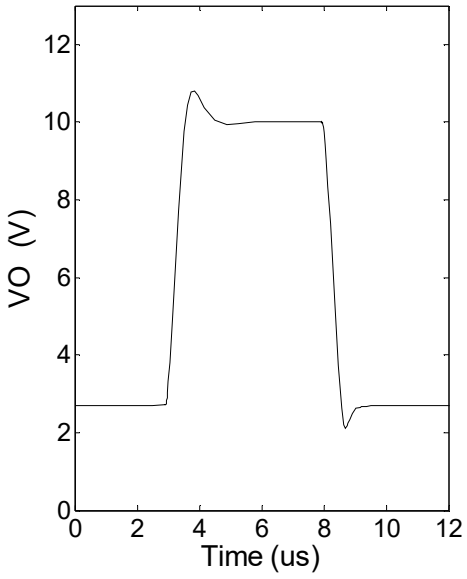


Figure 4.13. Output of the opamp in source follower configuration driving a 1 nF capacitor.

Table 4.1. Summary of the SiC JFET opamp performance parameters for V_{dd} = 15 V, V_{ss} = 0 V, CC = 12 nF, RZ = 20 Ω, C-Load = 1 nF, and T = 26°C.

Performance Parameters of the Opamp	
Open loop gain	67 dB
Unity gain frequency	2.68 MHz
Phase margin	43°
CMRR	73 dB
PSRR+, PSRR–	78 dB, 76 dB
Slew rate (rising), Slew rate (falling)	17.1 V/us, 15.4 V/us
ICMR	3.1 V to 10.6 V
Output resistance	28 Ω

4.4 High Temperature Design Consideration in DC Domain

The gain reduction of an amplifier stage at elevated temperature is a significant challenge (in DC domain) for an opamp design. The simulation result of the opamp in the range of 27°C to 350°C shows a large DC gain degradation (about three to four times), which can be partially compensated by additional circuitry. A simple biasing circuit was used in the original design, where it was not reflecting appropriate biasing to the amplification stages over the range of 27°C to 350°C. In order to maintain the appropriate biasing, an adaptive bias circuit needs to be designed and connected to V_{bias} in figure 4.14. This adaptive bias circuit is required to provide approximately one volt increase, when temperature increases from 27°C to 350°C.

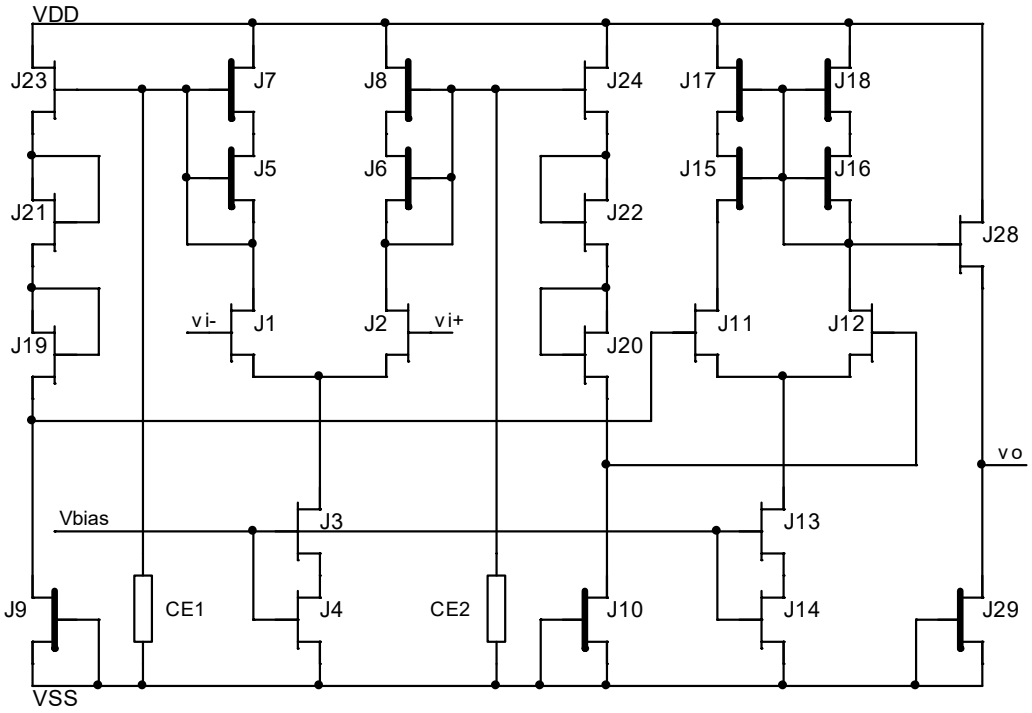


Figure 4.14. An adaptive DC biasing circuit can be designed for V_{bias} to partially compensate the gain reduction over the temperature range of 27°C to 350°C.

4.5 Conclusion

The main goal of this chapter to demonstrate the feasibility of a SiC JFET-based opamp is achieved. In the design flow, first, SiC JFET devices are characterized and modeled for SPICE and simulation. The design objective was to overcome the low intrinsic gain issues of the amplifiers and improve overall gain and CMRR performance of the opamp in a way that low GSVR requirement is considered. This is accomplished by using two diffamps, the first one using self-biased cascoded loads and the second one using the bootstrapping technique. Diffamp2 is used to not only set the overall gain and improve the CMRR performance, but also to meet the low GSVR requirement. The final

design test result confirms that the design objective is achieved. As the fabrication technology for SiC devices is improving, perfectly matched and smaller size devices will be developed to reduce offsets and improve the opamp's bandwidth.

CHAPTER V

OPERATIONAL AMPLIFIER DESIGN BASED ON SILICON CARBIDE JFET FOR OVERALL PERFORMANCE

5.1 Introduction

Superior performance of the SiC semiconductor such as SiC JFETs for high temperature and harsh environment is widely known. However, utilizing SiC JFET for analog design exhibits significant design challenges, even at room temperature. These fundamental challenges are low intrinsic gain, low GSVR requirement, and restriction utilizing CL as a design parameter due to fabrication complexity. First, these challenges must successfully be overcome in room temperature to be able to present any high temperature SiC JFET-based analog design. The main objective of this chapter is to overcome the design challenges, demonstrate the feasibility, and present an all SiC JFET transistors based opamp that is designed for reliability and overall performance. Before attempting to design, EM and DM SiC JFETs are characterized, analyzed, and modeled for simulation. A unique and reliable four stage opamp configuration is presented that takes design requirements into account, uses threshold voltage instead of CL as a design parameter, and employs gain enhancing design techniques while obtaining maximum possible bandwidth in a two stage opamp. The final opamp is fabricated and tested where 66.7 dB open loop gain and 5.71 MHz unity gain frequency are reported.

5.2 Circuit Configuration and Description

Overall configuration of the opamp, shown in figure 5.1, contains four stages and two CEs, CE1 and CE2, capable of driving a 1 nF capacitive load. The main strategy of the overall design is to keep the number of the transistors at minimum. First stage, a diffamp, is followed by a Differential to Single-ended and Level Shifter (DSLS). A CG amplifier is employed as a third stage, which is seldom seen in the opamps. Usually a high gain CS amplifier is used as a second amplifier stage, but in the case with SiC JFET, low GSVR requirement of its driver transistor prevents from using that. A source degenerated CS amplifier configuration might be considered, but there will be a significant tradeoff between the gain and GSVR. Unlike a CS amplifier, GSVR requirement of the driver transistor in a CG amplifier can be easily maintained while having a configuration with high gain performance. A CG amplifier provides the opamp not only a high gain, but also a maximum achievable bandwidth in an opamp with two amplifier stages. In the final stage, a SF is used to deliver the amplified signal to the load.

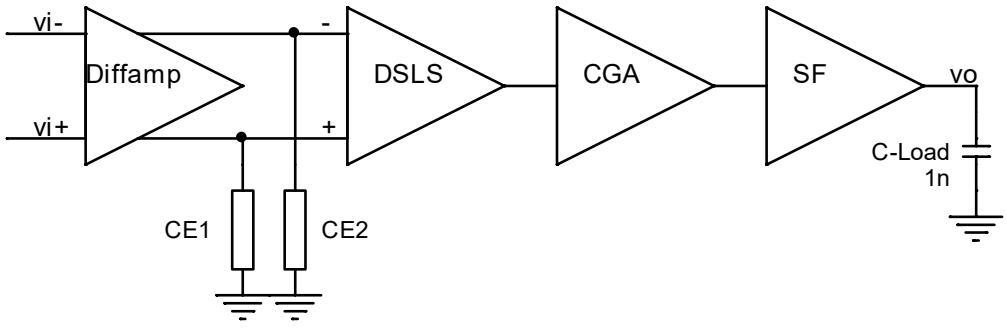


Figure 5.1. Circuit configuration of the opamp with external CE1 and CE2.

5.2.1 Differential Amplifier with Enhanced Cascoded Load

The first stage of the opamp in figure 5.2 is a diffamp using enhanced cascoded load configuration. It consists of four EM devices, J1 to J4 with V_{th} of +0.5, and four DM devices, J5 to J8 with V_{th} of –0.5, –0.5, –2, and –2 respectively. J3 and J4 are cascoded

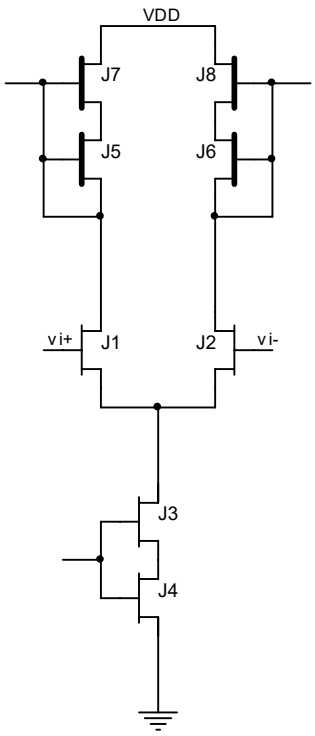


Figure 5.2. First stage amplifier, diffamp, with enhanced cascoded loads.

EM devices in order to have higher tail output resistance and better CMRR. Figure 5.3 shows that the diffamp produces –28 V/V voltage gain with an offset voltage of 59 mV associated with drivers and load transistor mismatches. The fabrication technology for SiC devices, and more specifically SiC JFETs, is still evolving, and design

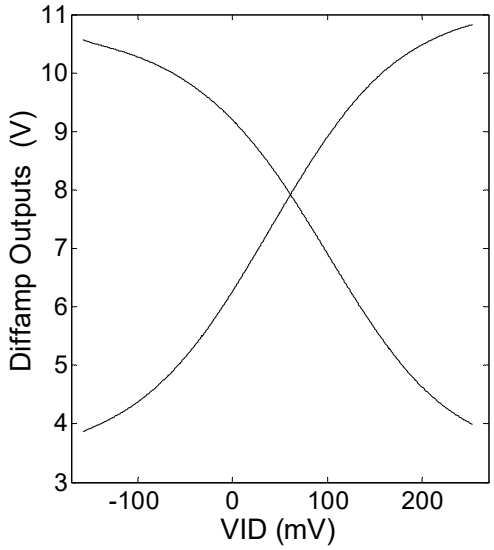


Figure 5.3. Measured transfer curves of the diffamp with gain of –28 V/V.

should accommodate larger tolerances for devices. The small signal differential gain equation of the diffamp is presented in equations (1) and (2). The frequency response of the diffamp in figure 5.4 shows a cutoff frequency of 610 KHz and unity gain frequency of 23 MHz. These devices were designed and fabricated for high current and power electronics applications. Their gate to drain and gate to source areas are very large, accordingly, so are their associated parasitic capacitances. By inspecting the structure of

$$A_{v_1} = \frac{v_{d1}}{v_{g1} - v_{g2}} = \frac{-g_{m1} r_{o1} (r_{o5} + r_{o7} + g_{m7} r_{o5} r_{o7})}{2(r_{o1} + r_{o5} + r_{o7} + g_{m7} r_{o5} r_{o7})} \quad (1)$$

$$A_{v_2} = \frac{v_{d2}}{v_{g1} - v_{g2}} = \frac{g_{m2} r_{o2} (r_{o6} + r_{o8} + g_{m8} r_{o6} r_{o8})}{2(r_{o2} + r_{o6} + r_{o8} + g_{m8} r_{o6} r_{o8})} \quad (2)$$

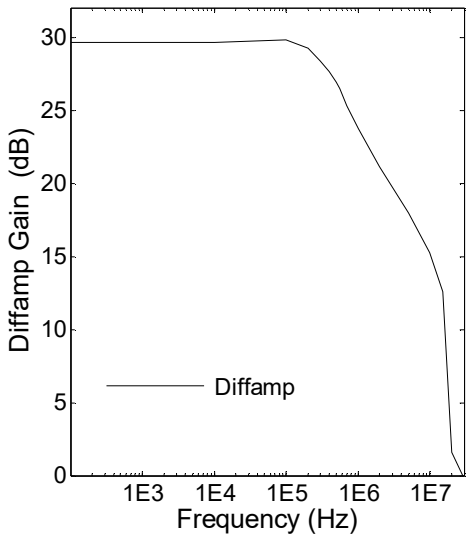


Figure 5.4. Measured frequency response of the diffamp.

these devices, it can be realized that the area between gate to drain is even larger than the area between gate to source. These two reasons explain the limitation seen in the diffamp's measured bandwidth. However, the design can scale to higher bandwidth with use of smaller transistors.

5.2.2 Differential to Single Ended and Level Shifter

The second stage in figure 5.5, DSLS of the opamp containing eight EM transistors, J9 to J16 with V_{th} of 0.5 V, plays an essential role in the entire design. It delivers a preamplified signal to the second stage amplifier and converts a differential input signal to a single ended output. DSLS also biases the second gain stage and ensures that the GSVR requirement of the driver transistor in CG amplifier is preserved. Four diode connected EM transistors, J13 to J16, not only level shift the output signal but also

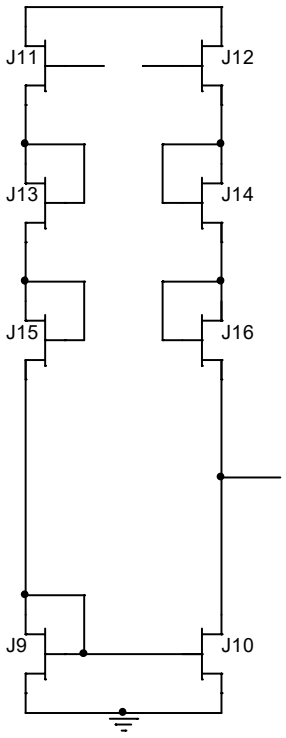


Figure 5.5. DSLS stage to convert differential inputs to single ended output along with level shifting.

maintain the GSVR requirement of the J9 and J10 transistors. Using figure 5.6(a) and (b), small signal analysis of the DSLS is conducted, where differential and common mode gains of the DSLS are calculated and shown in equations (3) and (4). Considering these equations, differential and common mode gains are 1.16 and 0.19 V/V, respectively.

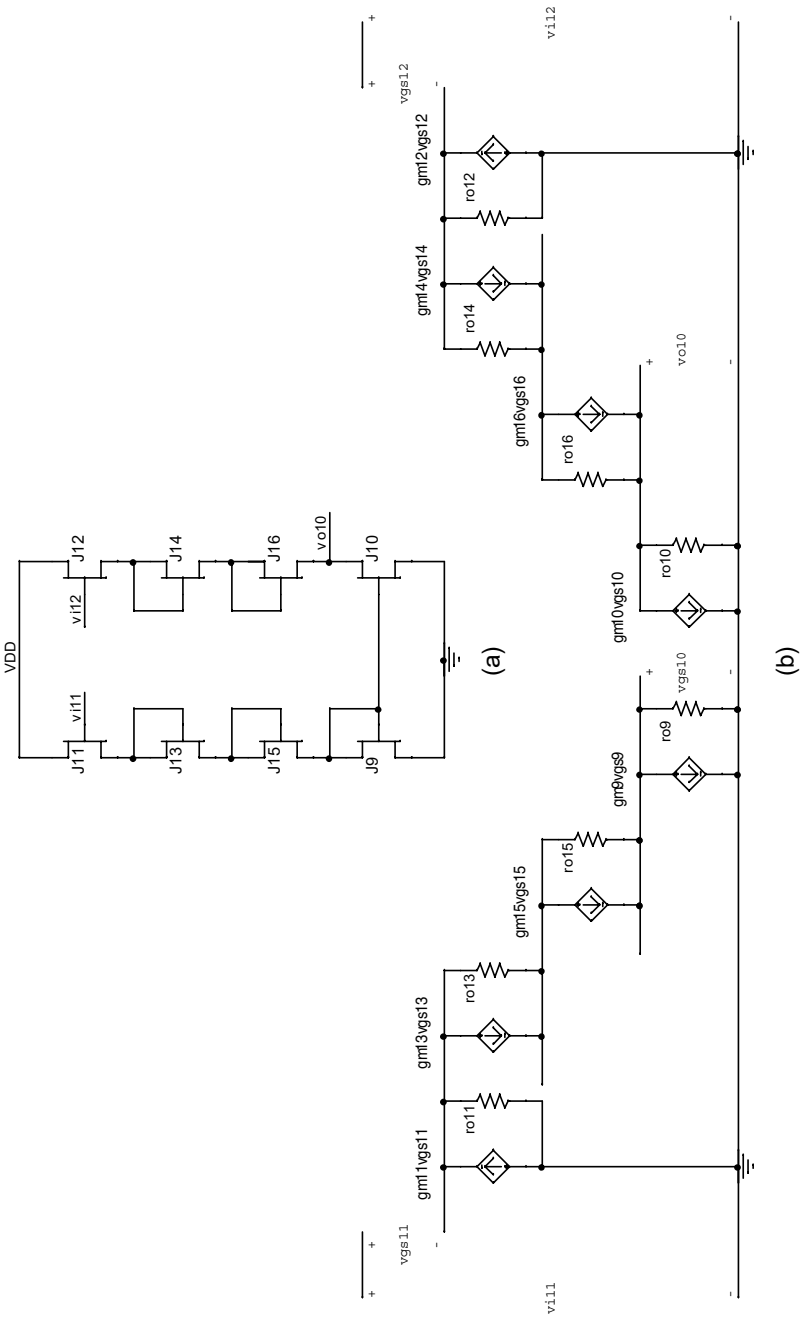


Figure 5.6. (a) DSLS. (b) Small signal equivalent of the DSLS to calculate differential and common mode gain.

$$A_{v_{diff}} = \frac{g_{m12}\left(g_{m11} + g_{m9} + \frac{1}{r_{o11} // r_{o9}} + r_d \cdot p\right) + g_{m11}g_{m10}(1 + r_d \cdot q)}{2\left(g_{m11} + g_{m9} + \frac{1}{r_{o11} // r_{o9}} + r_d \cdot p\right)\left(g_{m12} + \frac{1}{r_{o10} // r_{o12}} + \frac{r_d}{r_{10}} \cdot q\right)} \tag{3}$$

$$A_{v_{cm}} = \frac{g_{m12}\left(g_{m11} + g_{m9} + \frac{1}{r_{o11} // r_{o9}} + r_d \cdot p\right) - g_{m11}g_{m10}(1 + r_d \cdot q)}{2\left(g_{m11} + g_{m9} + \frac{1}{r_{o11} // r_{o9}} + r_d \cdot p\right)\left(g_{m12} + \frac{1}{r_{o10} // r_{o12}} + \frac{r_d}{r_{10}} \cdot q\right)} \tag{4}$$

$$p = \left(\frac{1 + g_{m11}r_{o11} + g_{m9}r_{o9} + g_{m11}g_{m9}r_{o11}r_{o9}}{r_{o11}r_{o9}}\right); \; q = \left(g_{m12} + \frac{1}{r_{o12}}\right);$$

$$r_d = \frac{1}{g_{m13} + \frac{1}{r_{o13}}} + \frac{1}{g_{m15} + \frac{1}{r_{o15}}} = \frac{1}{g_{m14} + \frac{1}{r_{o14}}} + \frac{1}{g_{m16} + \frac{1}{r_{o16}}}$$

$$\frac{A_{v_{diff}}}{A_{v_{cm}}} = \frac{g_{m12}\left(g_{m11} + g_{m9} + \frac{1}{r_{o11} // r_{o9}} + r_d \cdot p\right) + g_{m11}g_{m10}(1 + r_d \cdot q)}{g_{m12}\left(g_{m11} + g_{m9} + \frac{1}{r_{o11} // r_{o9}} + r_d \cdot p\right) - g_{m11}g_{m10}(1 + r_d \cdot q)} \tag{5}$$

From equations (3) and (4), differential to common mode gain ratio of equation (5) can be obtained, which is 6.1 V/V. The CMRR of the opamp is mainly determined by the diffamp; however, the DSLS is contributing to the overall CMRR. It should be mentioned that the number of diode connected EM transistors can determine the amount of the level shifting, differential to common mode gains ratio, and the amount of the output voltage swing. In other words, when the number of these diodes increases both

differential and common mode gains decrease, but common mode gain decreases more rapidly resulting in an increase in the differential to common mode gains ratio, which is a desirable effect. For example, using these four diode connected transistors in figure 5.5 resulted in an increase of 17 % in the differential to common mode gains ratio compared to using only two diode connected transistors. If no diodes are used, DSLS becomes simplified [23], voltage swing becomes maximized, and equations reduce to (6) and (7). This is not recommended, since J9 and J10 will be overstressed under excessive GSVR.

$$A_{v_{diff}} = \frac{g_{m12}\left(g_{m11} + g_{m9} + \frac{1}{r_{o11} // r_{o9}}\right) + g_{m11}g_{m10}}{2\left(g_{m11} + g_{m9} + \frac{1}{r_{o11} // r_{o9}}\right)\left(g_{m12} + \frac{1}{r_{o10} // r_{o12}}\right)} \tag{6}$$

$$A_{v_{cm}} = \frac{g_{m12}\left(g_{m11} + g_{m9} + \frac{1}{r_{o11} // r_{o9}}\right) - g_{m11}g_{m10}}{2\left(g_{m11} + g_{m9} + \frac{1}{r_{o11} // r_{o9}}\right)\left(g_{m12} + \frac{1}{r_{o10} // r_{o12}}\right)} \tag{7}$$

5.2.3 Common Gate Amplifier

The third stage of the opamp is a CG amplifier in figure 5.7, providing a gain of +79.8 V/V that is shown in figure 5.8. This stage consists of a driver, J17 with V_{th} of +0.5, connected to the cascoded current source load configuration of figure 3.7(e), which provides a high output resistance. Equation (8) shows small signal gain of the amplifier. Transistors J25 to J28, DM devices with V_{th} of –0.5 V, are used as voltage dividers.

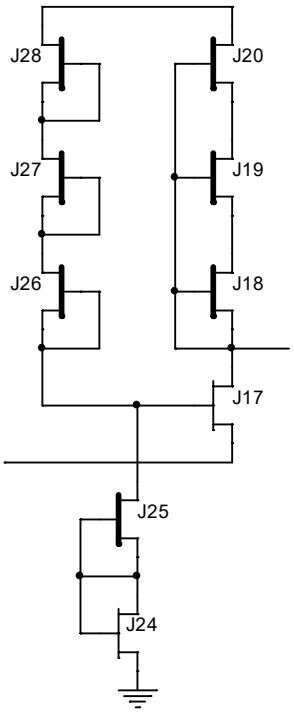


Figure 5.7. Second amplifier stage or CG amplifier.

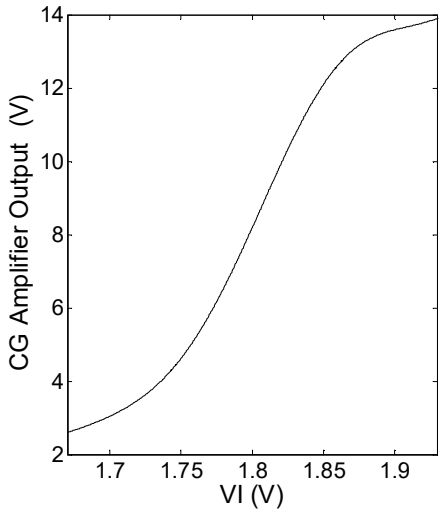


Figure 5.8. Measured transfer curves of the second amplifier stage, CG amplifier, with gain of +79.8 V/V.

$$A_{v_{CGA}} = (g_{m17} + \frac{1}{r_{o17}})(r_{o17} // r_{ol}) \tag{8}$$

$$r_{ol} = r_{o18} + r_{o19} + r_{o20} + g_{m19} r_{o18} r_{o19} + g_{m19} g_{m20} r_{o18} r_{o19} r_{o20} + g_{m20} r_{o20} (r_{o18} + r_{o19})$$

Transistor J24, an EM with V_{th} of +0.5 V, is used as a diode connected device to set the gate bias voltage for J17. In figure 5.9, the frequency response of the CG amplifier measures cutoff frequency of 490 KHz and unity gain frequency of 28 MHz. Gain Bandwidth Product (GBP) of the CG amplifier is greater than the CS amplifier, as expected. Additionally, a more relaxed GSVR requirement of the J17 in the CG amplifier provides the opamp with more reliability.

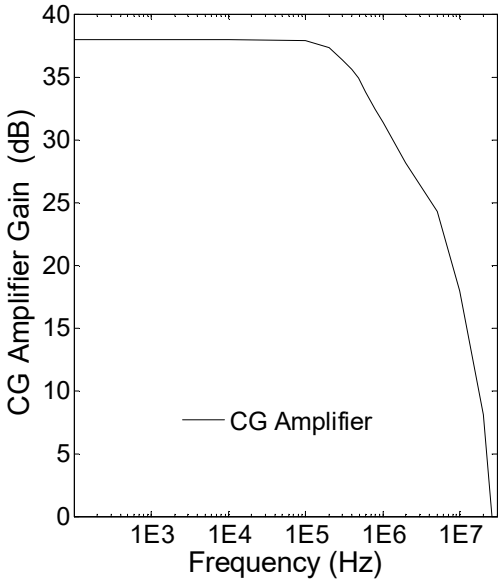


Figure 5.9. Measured frequency response of the CG amplifier.

5.2.4 Source Follower Stage

The fourth stage of the opamp is a SF, in figure 5.10, consisting of two EMs, J21 and J22 (V_{th} of +0.5), and a DM J23 with V_{th} of –1.5 V. This stage can supply 56 mA current and is capable of driving a 1nF capacitive load. Diode connected J22 is used to down level shift the output in order to ensure that the GSVR requirement of J1 and J2 are not violated when opamp is used in a feedback configuration. Equation (9) represents a small signal gain of the SF, which is less than unity.

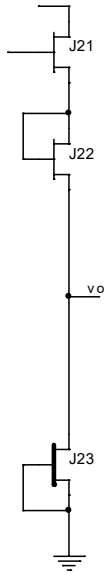


Figure 5.10. Output stage or SF.

$$A_{v_{SF}} = \frac{g_{m21}}{g_{m21} + \frac{1}{r_{o21} // r_{o23}} + \frac{r_{d22}}{r_{o23}} \cdot q} \tag{9}$$

$$r_{d22} = \frac{1}{g_{m21} + \frac{1}{r_{o22}}}, \quad q = g_{m21} + \frac{1}{r_{o21}}$$

5.3 Frequency Compensation of the Opamp

In order to provide the opamp with stability, the compensation scheme of figure 5.11 is used. In this opamp, other compensation schemes, such as Miller, nested Miller, etc., would not be practical because: there is no high gain inverting stage, and the aim is to avoid complexity and use minimum number of transistors. Figure 5.11 shows the first stage (diffamp) with and without compensation along with an ac model for stability analysis. Equations (10) and (11) show the frequency response of the diffamp without compensation. A pole associated with amplifier's input (a low frequency pole) and amplifier's output (a high frequency pole) and a right half plane zero created by gate to drain capacitances of the driver transistors J1 in (10) and J2 in (11) can be observed.

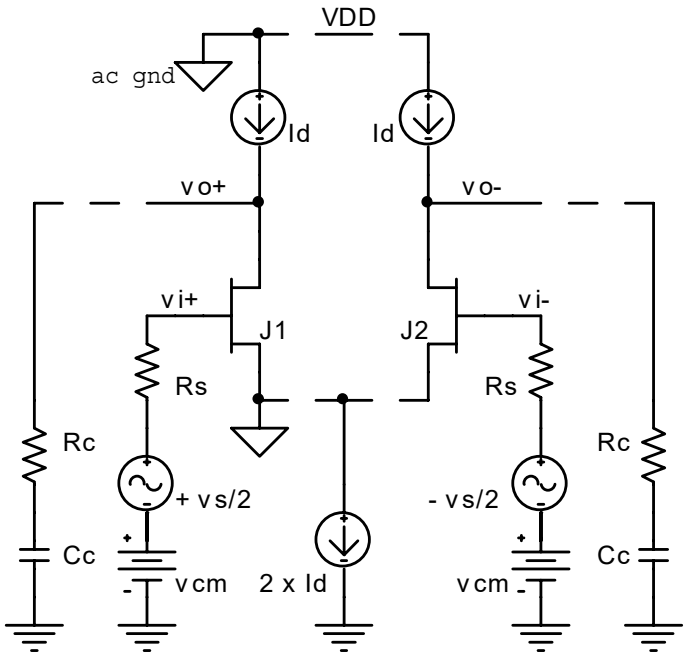


Figure 5.11. Diffamp and compensation scheme of the opamp.

$$\frac{v_{o+}}{v_s} = -\frac{1}{2} \cdot \frac{a_1 s + a_0}{b_2 s^2 + b_1 s + b_0}, \tag{10}$$

$$\frac{v_{o-}}{-v_s} = \frac{1}{2} \cdot \frac{a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} \tag{11}$$

$$a_0 = -g_m R_{out},\ R_{out} = r_{o1} // r_{o(Id)},$$

$$a_1 = R_{out} C_{gd},$$

$$b_0 = 1,$$

$$b_1 = \left[R_s C_{gs} + R_s C_{gd} \left(1 + R_{out} \left(\frac{1}{R_s} + g_m \right) \right) + R_{out} C_{ds} \right],$$

$$b_2 = R_s R_{out} (C_{gs} C_{gd} + C_{gs} C_{ds} + C_{gd} C_{ds})$$

The right half plane zero has the same effect on the transfer function's phase response as a left half plane pole; consequently, the combination of a low frequency pole and a right half plane zero results in a 180° phase drop producing instability. In order to introduce stability to the opamp, compensation capacitors with series resistors are added to the outputs of the diffamp. Equations (12) and (13) demonstrate the frequency response of the amplifier with CE1 and CE2. Due to compensation, both a new dominant pole and a left half plane zero can be observed by inspecting the numerator and denominator coefficients of the transfer function.

$$\frac{v_{o+}}{v_s} = -\frac{1}{2} \cdot \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{12}$$

$$\frac{v_{o-}}{-v_s} = \frac{1}{2} \cdot \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{13}$$

$a_0 = -g_m R_{out}$, $R_{out} = r_{o1} // r_{o\,(Id)}$,

$a_1 = R_{out} C_{gd} - g_m R_{out} R_c C_c$,

$a_2 = R_{out} C_{gd} R_c C_c$,

$b_0 = 1$,

$$b_1 = \begin{bmatrix} R_s C_{gs} + R_s C_{gd} \left(1 + R_{out} (\frac{1}{R_s} + g_m) \right) + \\ R_{out} C_{ds} + (R_{out} + R_c) C_c \end{bmatrix},$$

$$b_2 = \begin{bmatrix} R_s C_{gs} C_c (R_{out} + R_c) + \\ R_s C_{gd} R_c C_c \left(1 + R_{out} (\frac{1}{R_s} + g_m) \right) + R_{out} C_{ds} R_c C_c + \\ R_s R_{out} R_c C_c (C_{gs} C_{gd} + C_{gs} C_{ds} + C_{gd} C_{ds} + C_{gd} C_c) \end{bmatrix},$$

$b_3 = R_s R_{out} R_c C_c (C_{gs} C_{gd} + C_{gs} C_{ds} + C_{gd} C_{ds})$

A Compensation capacitor (Cc) adds a new dominant low frequency pole to roll off the magnitude response before reaching to the previous low frequency pole. A Small series resistor (RZ) adds a new left half plane zero to control the effect of the right half plane zero. It reverses the phase drop created by the new pole and continues the reversal until reaching to the right half plane zero and the next pole (a high frequency pole). Therefore, phase response of the amplifier maintains an appropriate phase margin, introducing stability to the opamp.

5.4 Complete Opamp and Results

Final opamp of figure 5.12 contains all the described stages plus a bias stage setting appropriate tail current for diffamp to obtain maximum differential gain. Since the

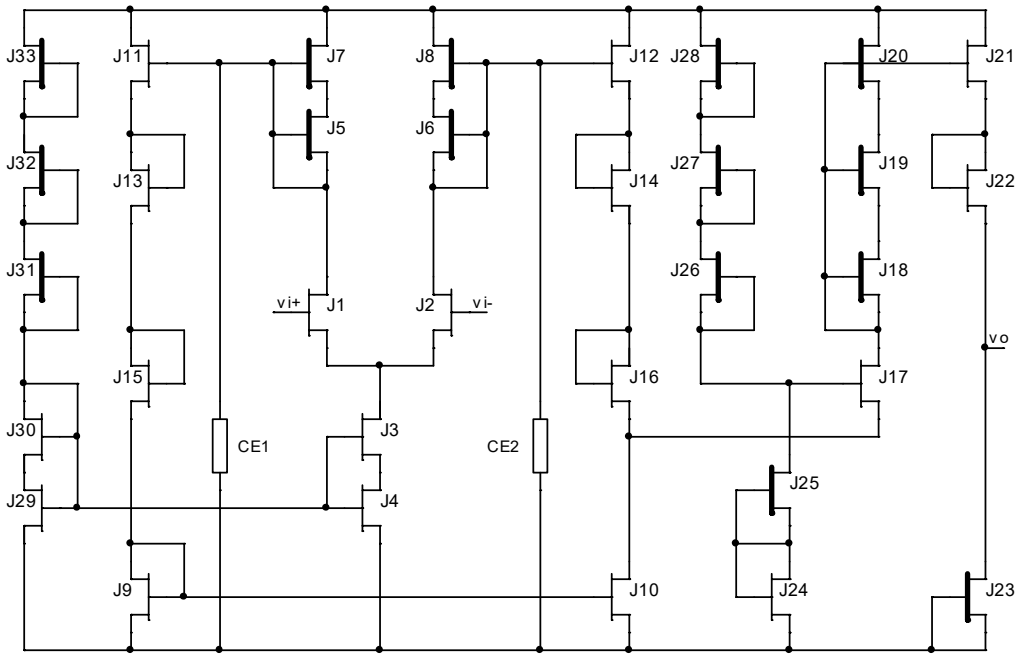


Figure 5.12. Complete schematic of the opamp.

GVSR requirement of J1 and J2 is also depended on the tail bias current, the current can be reduced to relax the GSVR requirement at the expense of maximum differential gain reduction. By relaxing the GSVR requirement, higher ICMR for the entire opamap can be obtained. The final design shown in figure 5.12 is fabricated, packaged, and tested. Since fabrication of SiC JFET based circuits is in its infancy, having non idealities, such as large mismatches and offsets, are expected. The final opamp is fabricated by integrating forty dies on an aluminum nitride substrate and wire bounding the connections. Each die is 650 μm by 650 μm containing four transistors. Every stage, along with the entire opamp, is both simulated and tested. In the device modeling process, devices are modeled to reflect slightly worse small signal characteristics than their actual measured characteristics; therefore, test results always showed slightly better performance than the simulation results. Performance parameters of this opamp are shown in figure 5.13 through 5.16, and table 5.1. In table 5.1, performance parameters of the current work are compared with the work of the chapter four. Chapter four's work was focused on gain and CMRR, while this work emphasizes on a universal design for overall performance with improved reliability and relaxed GSVR requirements. Moreover, table 5.1 shows that GBP and slew rate of the current design are improved significantly. Improvement in GBP is a direct result of using a CG amplifier for the second amplifier stage. It should be mentioned that J1, J2 are not protected, and constant high GSVR (above maximum ICMR) can cause device overheating and reduction of their functional life time. The fabricated opamps of the chapter four and this chapter are shown in figure 5.17. Figure 5.18 illustrates the opamps and a fabricated board for testing purposes.

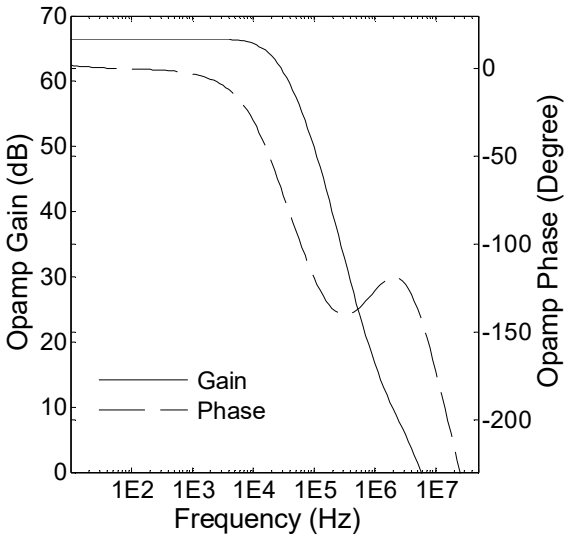


Figure 5.13. Frequency and phase (dashed line) response of the final opamp.

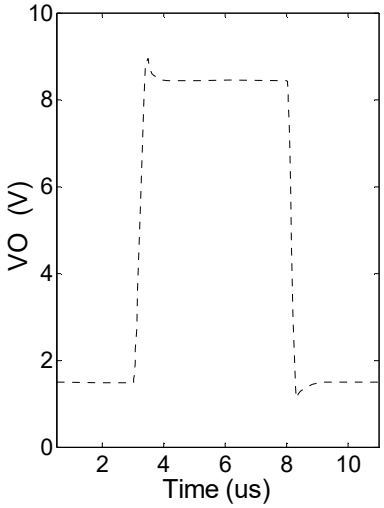


Figure 5.14. Output of the opamp driving a 1nF capacitive load.

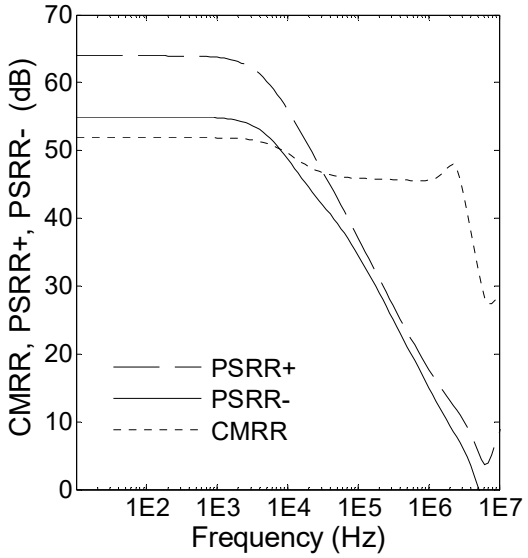


Figure 5.15. CMRR, PSRR+, and PSRR- performance of the opamp.

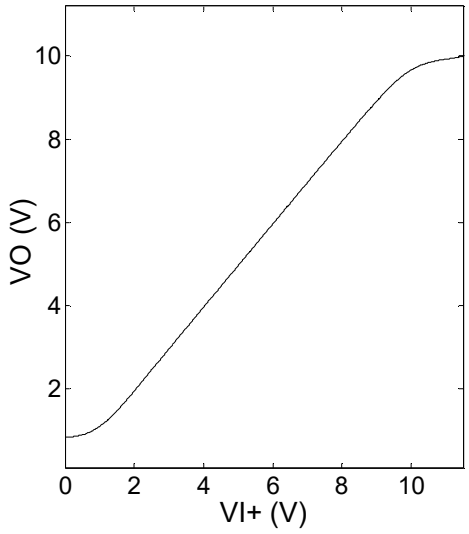


Figure 5.16. ICMR performance of the opamp.

5.5 Conclusion

Finally, design of a novel, fully SiC JFET-based opamp with unique and reliable configuration is presented. The design had to overcome three major challenges imposed by SiC JFETs: low intrinsic gain, low GSVR requirement, and restriction utilizing CL as a design parameter due to fabrication complexity. Before designing the opamp, device characteristics of both EM and DM type are characterized and modeled for simulation. Also, their capabilities and measured small signal characteristics for analog design are analyzed. In designing the opamp, a diffamp with improved cascoded current source load, a reliable DSLS, a CG amplifier for overall gain and reliability, and a first stage compensation scheme are presented. The performance parameters of the fabricated final

Table 5.1. Performance parameters summary of the current SiC JFET opamp compared with chapter four's opamp.

Parameters	**Chapter Four's Work** [1]	**Current Work** [2]
Open loop gain	67 dB	66.7 dB
Unity gain frequency	2.68 MHz	5.71 MHz
Phase margin	43°	46°
CMRR	73 dB	52 dB
PSRR+	78 dB	64 dB
PSRR–	76 dB	55 dB
ICMR	3.1 V to 10.6 V	1.2 V to 9.3 V
Slew rate (rising)	17.1 V/us	25.8 V/us
Slew rate (falling)	15.4 V/us	34.6 V/us
Output resistance	28 Ω	36 Ω

[1] V_{dd} = 15 V, V_{ss} = 0 V, CC = 12 nF, RZ = 20 Ω, C-Load = 1 nF, and T = 26°C.

[2] V_{dd} = 15 V, V_{ss} = 0 V, CC = 3.5 nF, RZ = 55 Ω, C-Load = 1 nF, and T = 26°C.

design confirm the feasibility of employing SiC JFETs in analog design. The opamp's performance will be improved, in the future, as the fabrication process and technology are being perfected. Perfect matched devices with smaller feature size will reduce offsets and improve the opamp's bandwidth.

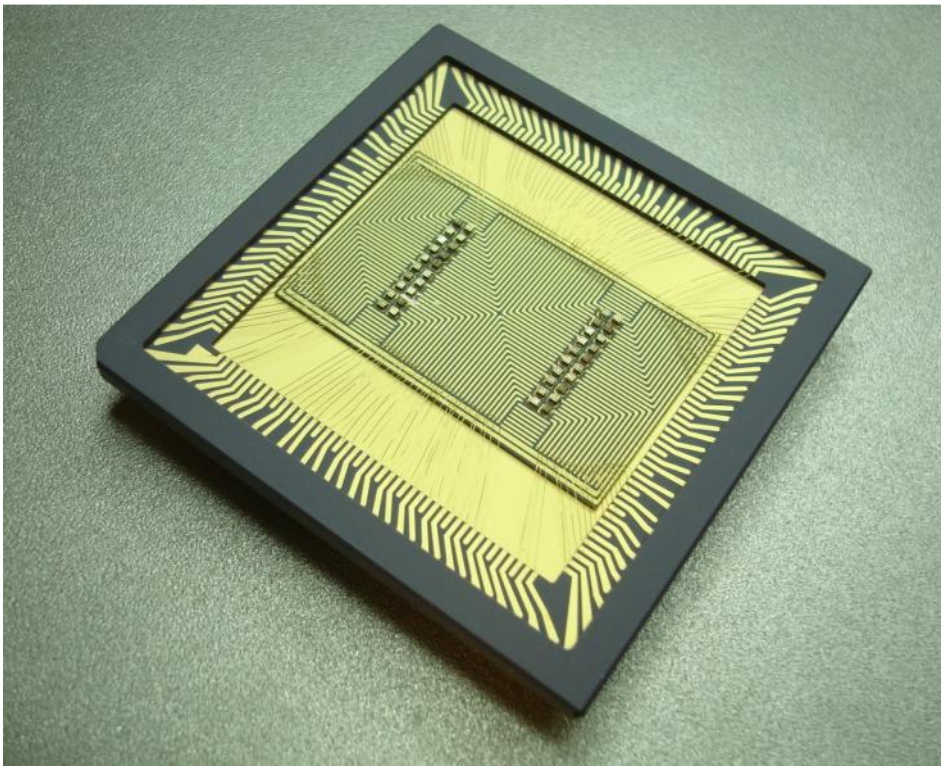


Figure 5.17. Fabricated, packaged, and tested fully EM and DM SiC JFET-based opamps.

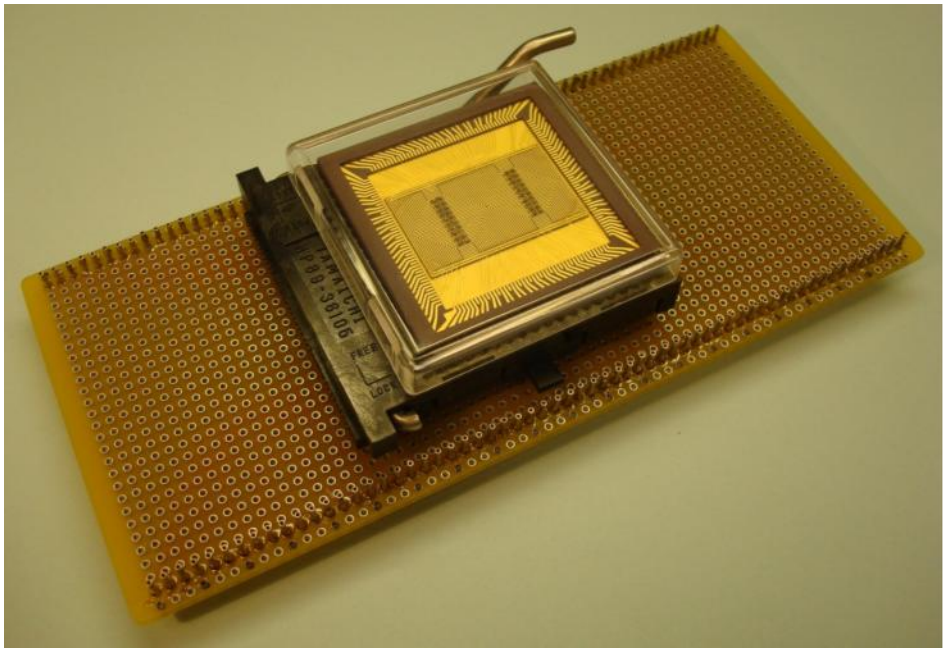


Figure 5.18. Opamps and a fabricated test board.

CHAPTER VI

CONCLUSION

The main objective of this research is accomplished: 1) Established a design baseline utilizing EM and DM SiC JFET devices for analog design. 2) Overcame the analog design challenges and requirements imposed by the devices. 3) Demonstrated the feasibility of all SiC JFET-based opamps by proposing two novel designs. 4) Presented all SiC JFET-based opamps that are designed, fabricated, and tested and their performances are reported.

Superior performance of the SiC JFET at both high temperature and in power electronics has been one of the major motivations behind development of SiC-based circuits in both analog and digital domains. Such development is currently in the stage of research because devices require optimization, circuit design approaches need to be established, and technology and fabrication challenges need to be conquered. The focus of this research was to explore and address the challenges in the design of the opamps that utilize existing Vertical Channel EM and DM 4H-SiC JFETs fabricated and provided for this research by SemiSouth Laboratories, Inc. After characterization of the devices, a number of design challenges is identified in the analog domain that is significant, even at room temperature. As a matter of fact, reliable high temperature SiC JFET-based circuits will only be possible if, as the first step, a reliable SiC JFET-based design at room

temperature exists. In order to pave the road for future work that might mainly focus on high temperature design, this research addressed design challenges at elevated temperature in the DC domain, as an initial step.

In chapter two, device characterization is used for modeling and SPICE simulation from 27°C to 400°C. In the device modeling, the already developed GaAs FET level five SPICE model is employed because our emphasis is analog circuit design appropriate to SiC JFETs rather than device-specific modeling. At any stage of the design, the test results are slightly better than the simulation results, which confirm that the modeling is reasonable and does not overestimate the performance. Although the modeling is quiet accurate at room temperature, but the accuracy of the modeling decreases as temperature increases. In other words, this model requires additional developments for higher temperature design. At the end of the chapter, the effect of temperature on V_{th}, transconductance, and output resistance of the SiC JFETs is explored, which shows that the intrinsic gain and V_{th} of the devices decrease at elevated temperature.

Analog building blocks and their performance analysis are reported in chapter three. In this chapter, device characteristics are explored to present design essentials for SiC JFET-based analog design. Based on the structural similarity between the EM and DM devices (which only differ in V_{th}) small signal parameters, such as transconductance and output resistance, are measured and compared. In applications that require higher gain rather than large GSVR, EM devices are best suited. In designs where large GSVR is critical, DM devices will perform better. Obviously, the trade off for a large GSVR

using DM devices is a low gain performance. Finally, the effect of temperature on a CS amplifier shows that the gain performance reduces to approximately 50 % from 27°C to 350°C.

In chapter four, an opamp is designed, fabricated, and tested for maximal gain and CMRR performance at room temperature. Design challenges are taken into consideration and solutions are found. The low intrinsic gain issue is solved by using cascoded DM devices as a current source and a compact high gain second stage in bootstrapped configuration. The requirement to limit the GSVR is taken into account by using EM devices in diode configuration for biasing purposes. Restrictions on utilizing CL as a design parameter due to fabrication complexity are resolved by using V_{th} parameter of the devices instead. The performance of the final opamp shows 67 dB of open loop gain and 73 dB of CMRR.

In chapter five, a more universal opamp is designed, fabricated, and tested. A novel design structure is presented that emphasizes on reliability and overall performance. In this design, the challenges are overcome in slightly different ways. The low intrinsic gain issue is solved by using cascoded DM devices with differing V_{th} to present an enhanced current source configuration. A CG amplifier structure, which is seldom used in opamps, is used to achieve high gain plus the maximum obtainable bandwidth in an opamp with two amplifier stages. The requirement to limit the GSVR is taken into account by using EM devices in diode configuration for biasing purposes and a CG amplifier that is capable of accepting higher GSVR. Restrictions on utilizing CL as a design parameter due to fabrication complexity are resolved by using V_{th} parameter of the

devices instead. The final opamp is fabricated and tested where 66.7 dB open loop gain and 5.71 MHz unity gain frequency are observed.

Finally, as mentioned earlier, device optimization of the SiC JFET will greatly improve the performance of the future opamps designed according to the methods first reported in this dissertation. Smaller device feature size to achieve higher bandwidth, fabrication technology improvements resulting in better matched devices with much lower offsets, and flexibility in adjusting CL in vertical channel devices are among the areas in which improvements will have a great impact on the performance of the future SiC JFET-based opamps.

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